

XRT Timeline to be uploaded on 2011/02/08

Period: 2011/02/08 10:10:00 - 2011/02/12 09:43:00

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Normal mode

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XOB #1858: HOP177 - Ti/Poly - Thin-Be - 384x512FOV - 2.5min cadence													
Term	Pointing (x, y)	Comment											
02/08 10:27:00 - 02/10 09:43:54	Track (-513.7, -540.4) ^{© 02/08 10:20:00}	# HOP 177 looking at South CH (OP start + 10min)											
PROG= 10 Inf.-time(s)													
└─ Subr= 1 1-time(s) 2.0sec													
└─ Seqn= 33 24-time(s) 150.0sec													
	Open/Ti-poly	Open/thick-Al	close	Safe	Norm	1.00s	Obs	1x1	384x512 (1024, 1024)	Q=95	3	0	2.0sec
	Open/Ti-poly	Open/thick-Al	close	Safe	Norm	4.00s	Obs	1x1	384x512 (1024, 1024)	Q=95	2	0	2.0sec
	thin-Be/Open	med-Be/Open	close	Safe	Norm	22.6s	Obs	1x1	384x512 (1024, 1024)	Q=95	0	0	2.0sec
└─ Seqn= 49 1-time(s) 2.0sec													
	thin-Be/Open	thin-Be/Open	close	Safe	Dark	22.6s	Obs	1x1	384x512 (1024, 1024)	DPCM	0	0	2.0sec
	Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)	Comp.	AEC Buffer	Interval	

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Flare mode

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XOB #1828: Flare Standard Obs. with eruptions mode-A (FW1=Open)													
Term	Pointing (x, y)	Comment											
02/08 10:27:00 - 02/10 09:43:54	Track (-513.7, -540.4) ^{© 02/08 10:20:00}	# HOP 177 looking at South CH (OP start + 10min)											
PROG= 16 1-time(s)													
└─ Subr= 1 30-time(s) 20.0sec													
└─ Seqn= 87 1-time(s) 2.0sec													
	Open/thick-Al	Open/thick-Al	close	Safe	Norm	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
	Open/thick-Be	Open/thick-Be	close	Safe	Norm	2.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└─ Seqn= 60 1-time(s) 2.0sec													
	Open/Al-mesh	Open/Al-mesh	close	Safe	Norm	125ms	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
	Open/Ti-poly	Open/Ti-poly	close	Safe	Norm	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
└─ Subr= 2 1-time(s) 2.0sec													
└─ Seqn= 90 1-time(s) 2.0sec													
	Open/G-band	Open/G-band	open	Safe	Norm	63ms	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=98	0	0	2.0sec
└─ Subr= 3 30-time(s) 60.0sec													
└─ Seqn= 87 1-time(s) 2.0sec													
	Open/thick-Al	Open/thick-Al	close	Safe	Norm	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
	Open/thick-Be	Open/thick-Be	close	Safe	Norm	2.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└─ Seqn= 88 1-time(s) 2.0sec													
	Open/Al-mesh	Open/Al-mesh	close	Safe	Norm	125ms	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
	Open/Ti-poly	Open/Ti-poly	close	Safe	Norm	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
└─ Subr= 2 1-time(s) 2.0sec													
└─ Seqn= 90 1-time(s) 2.0sec													
	Open/G-band	Open/G-band	open	Safe	Norm	63ms	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=98	0	0	2.0sec
└─ Subr= 3 30-time(s) 60.0sec													
└─ Seqn= 87 1-time(s) 2.0sec													
	Open/thick-Al	Open/thick-Al	close	Safe	Norm	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
	Open/thick-Be	Open/thick-Be	close	Safe	Norm	2.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└─ Seqn= 88 1-time(s) 2.0sec													
	Open/Al-mesh	Open/Al-mesh	close	Safe	Norm	125ms	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
	Open/Ti-poly	Open/Ti-poly	close	Safe	Norm	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
└─ Subr= 4 24-time(s) 600.0sec													
└─ Seqn= 89 1-time(s) 2.0sec													
	Open/Al-mesh	Open/thick-Al	close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)	Q=95	1	0	2.0sec
	Open/Ti-poly	Open/thick-Be	close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)	Q=95	1	0	2.0sec
	Open/G-band	Open/G-band	open	Safe	Norm	63ms	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Open/Al-mesh	Open/Al-mesh	close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
	Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)	Comp.	AEC Buffer	Interval	

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Active Region Search

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NOT USED

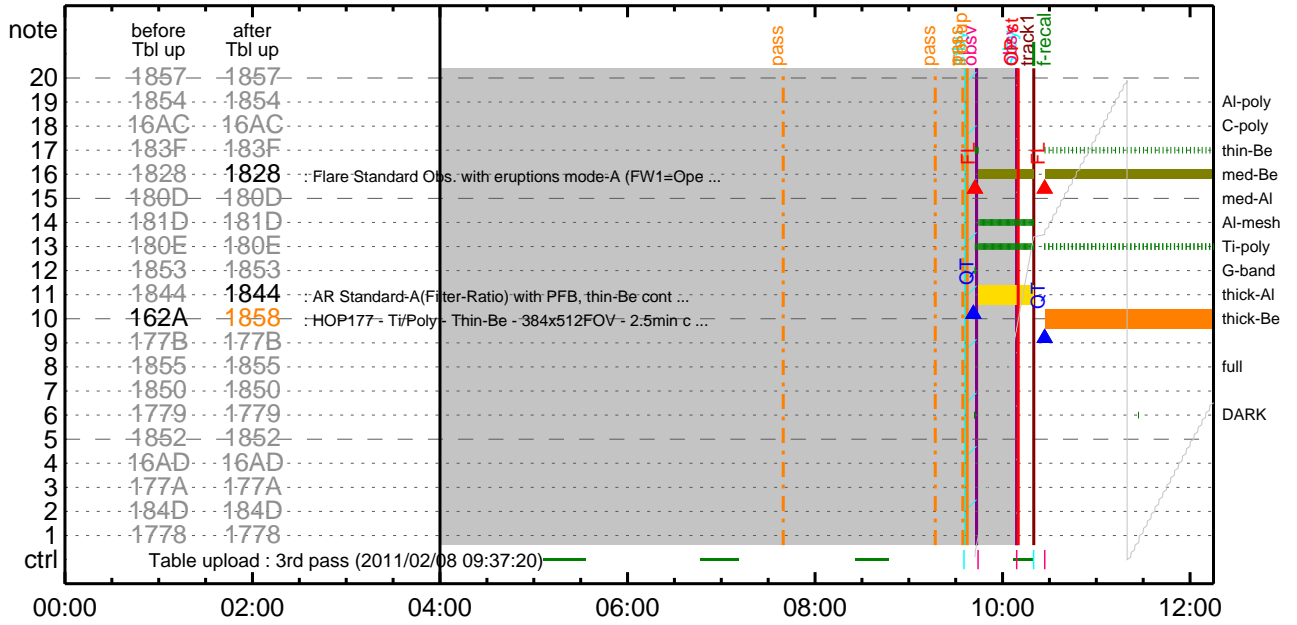
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Flare Detection

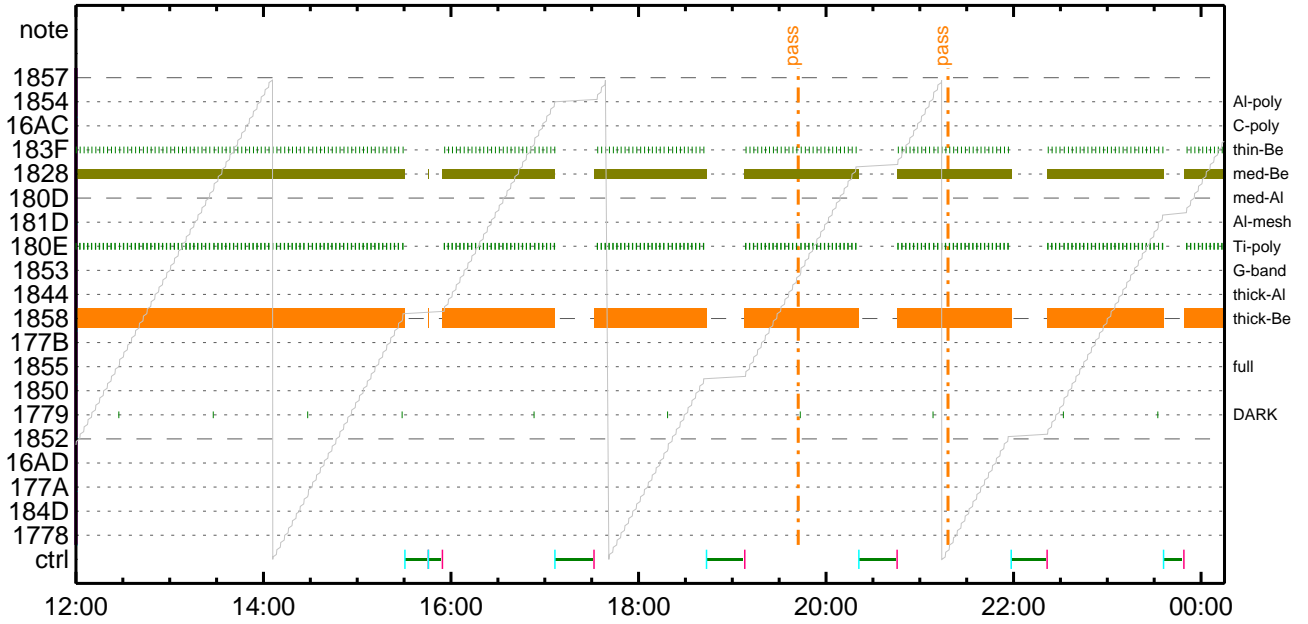
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NOT USED

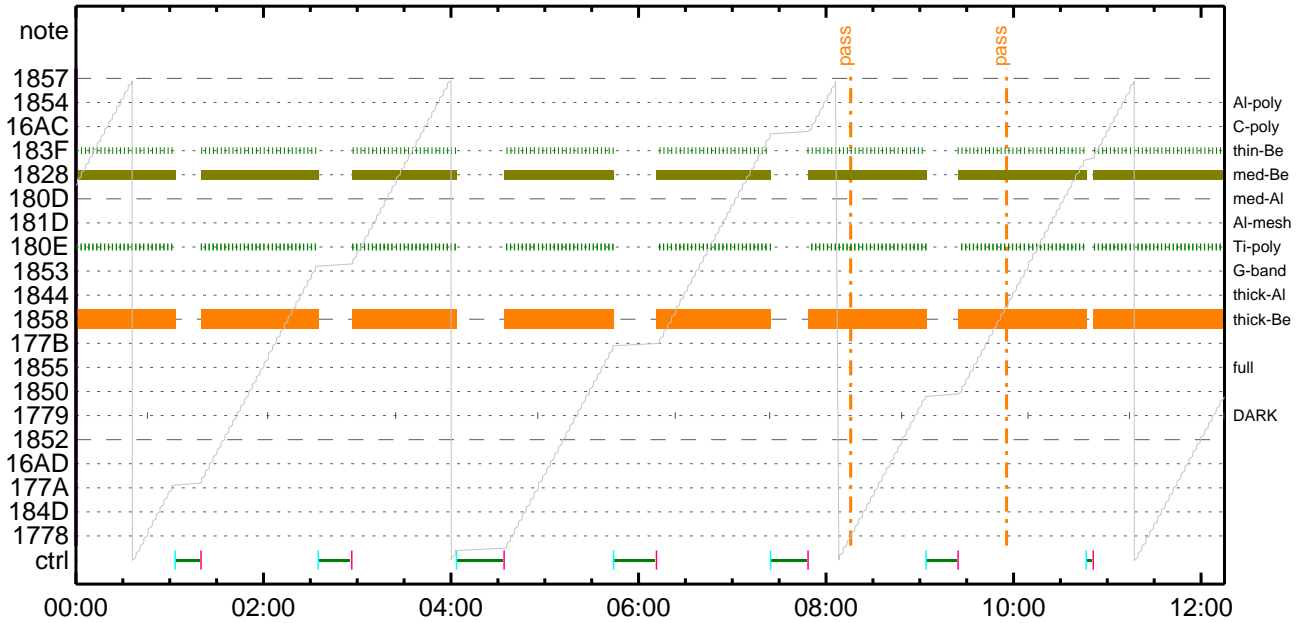
CMDI #0757 2011/02/08



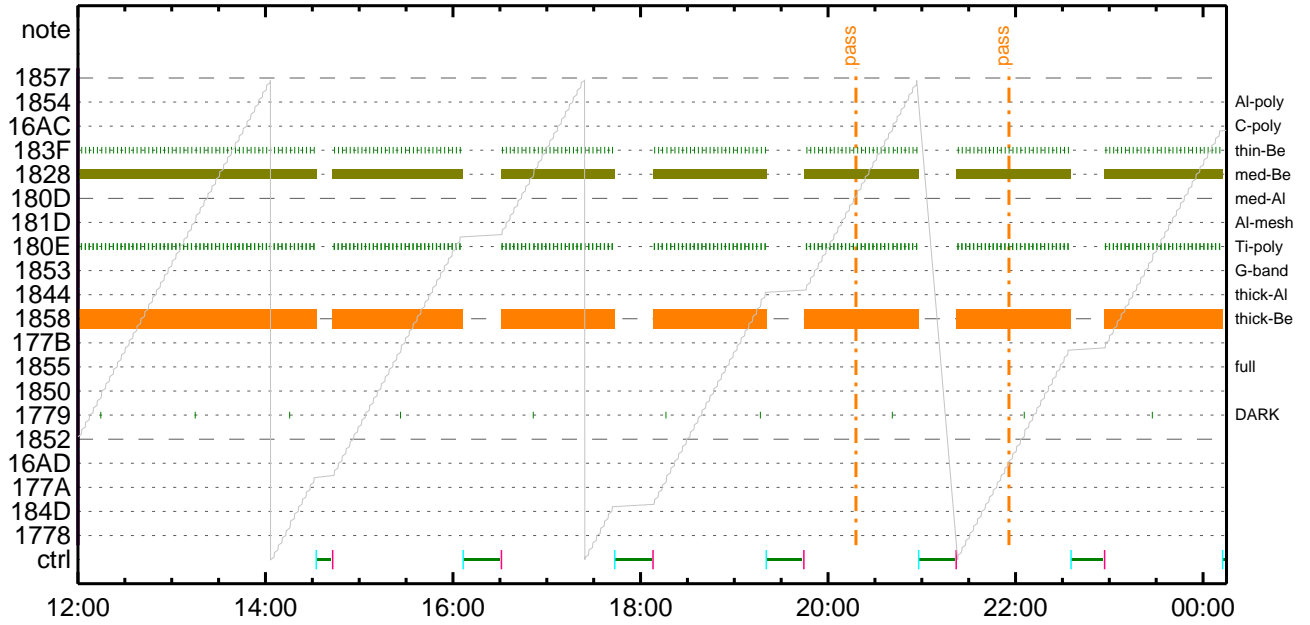
CMDI #0757 2011/02/08



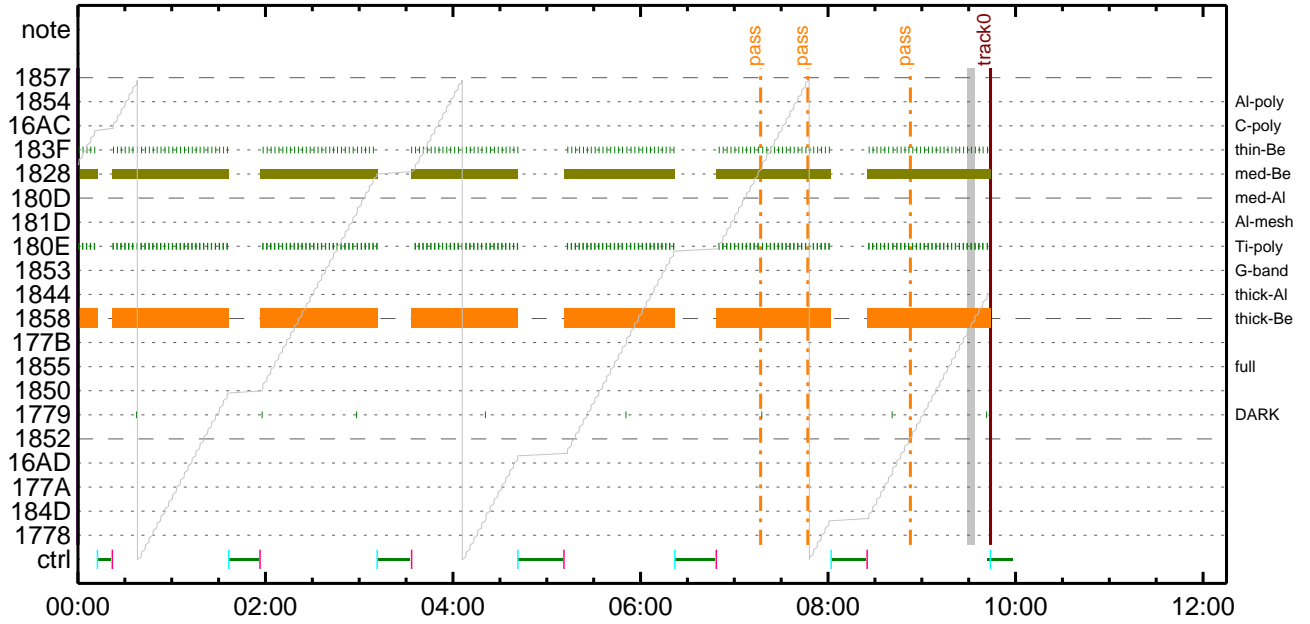
CMDI #0757 2011/02/09



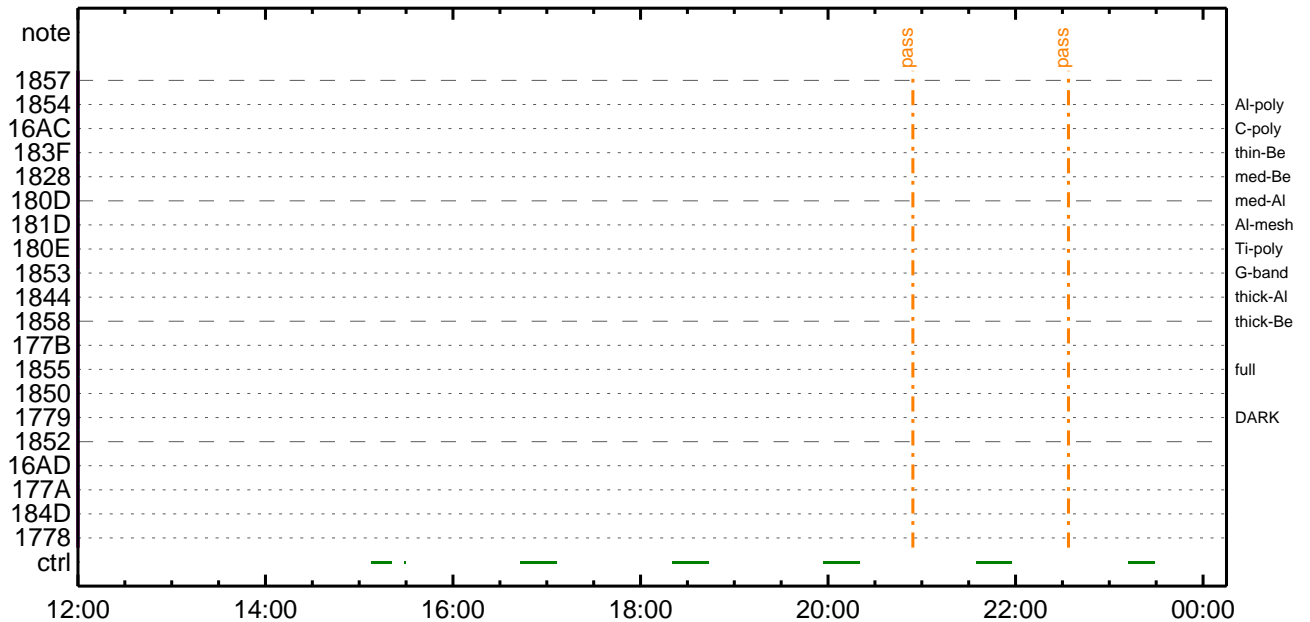
CMDI #0757 2011/02/09



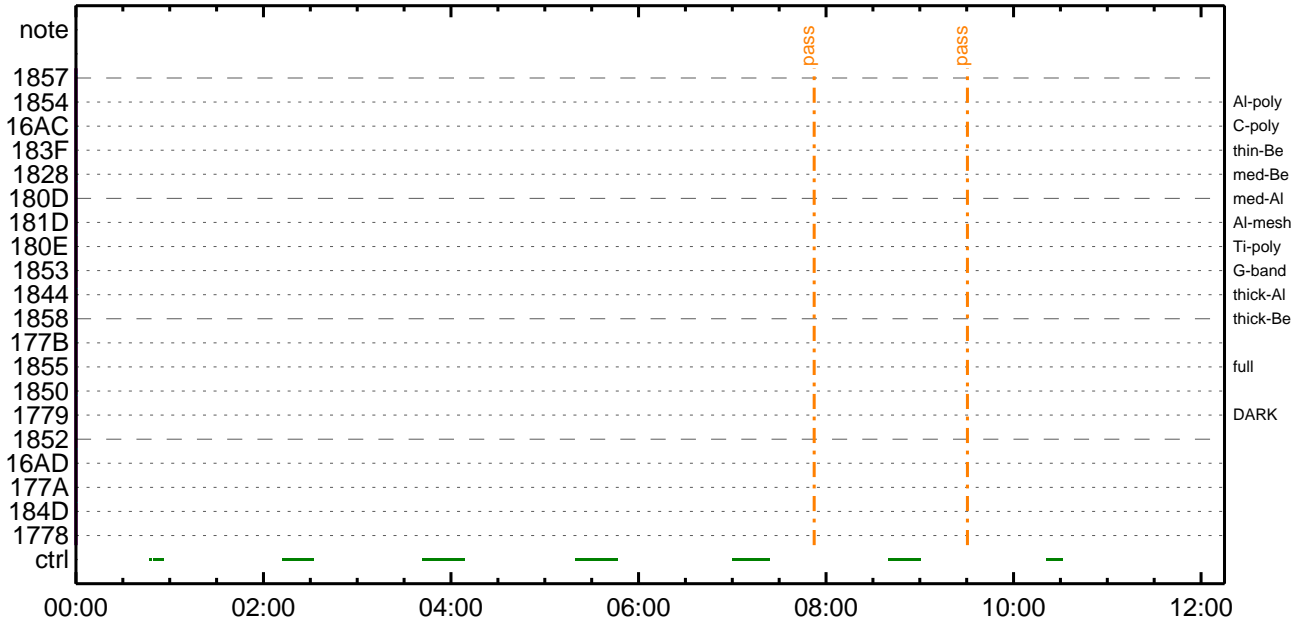
CMDI #0757 2011/02/10



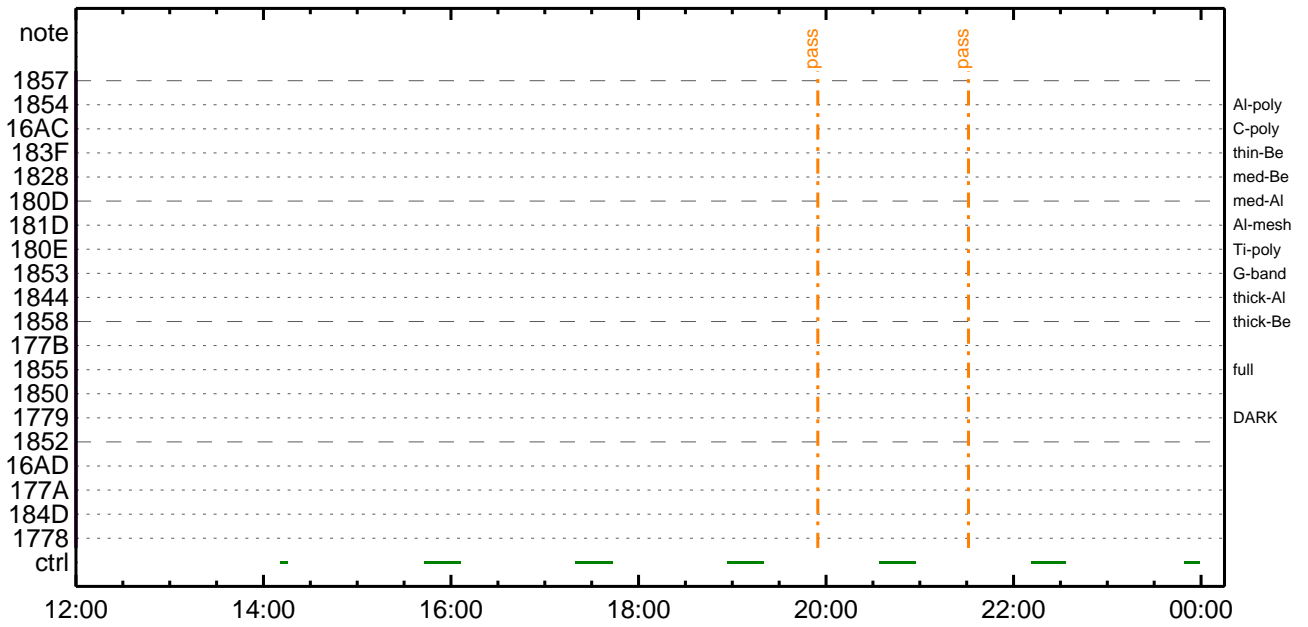
CMDI #0757 2011/02/10



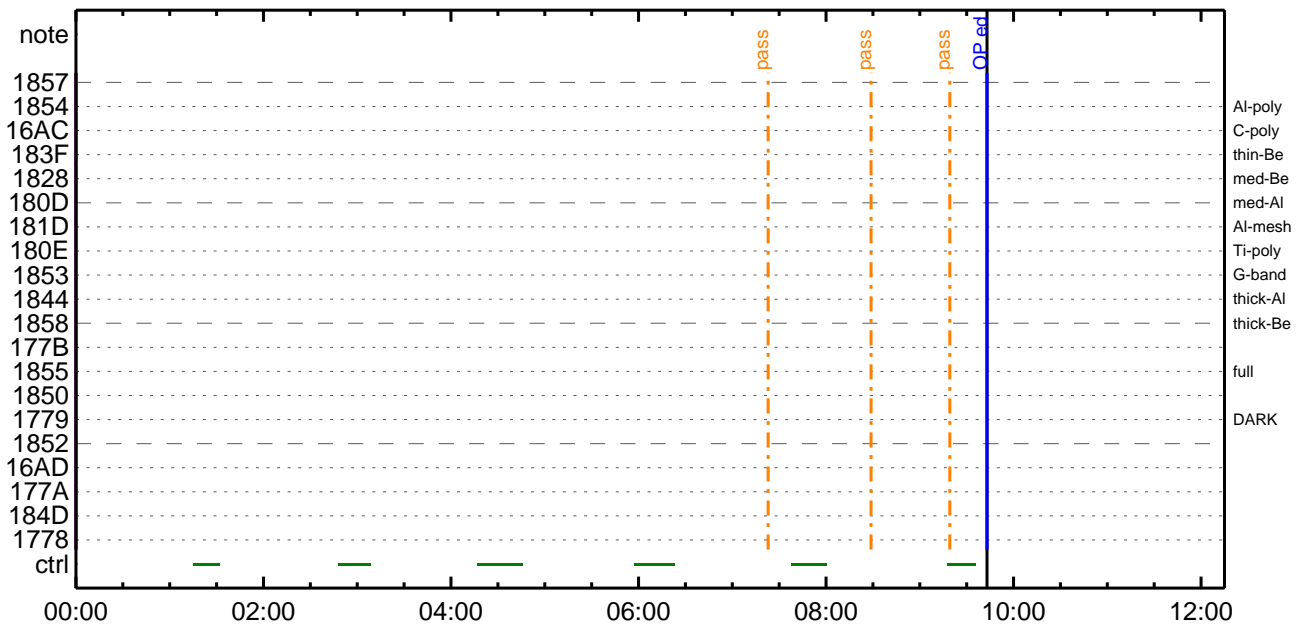
CMDI #0757 2011/02/11



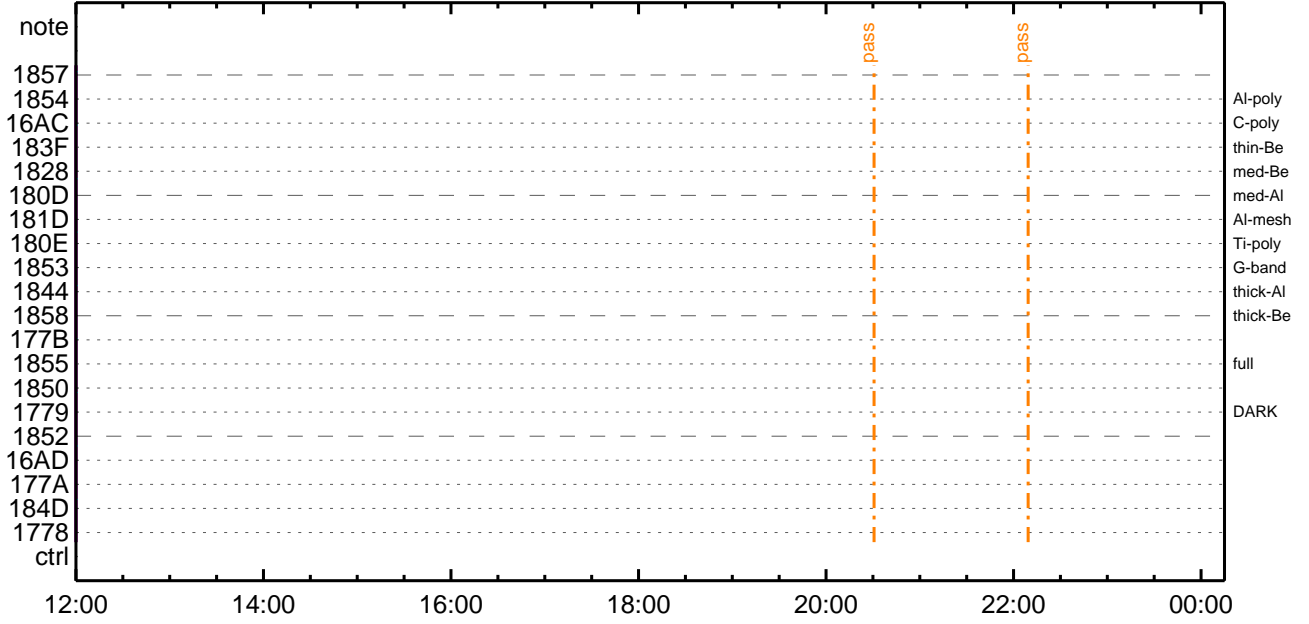
CMDI #0757 2011/02/11



CMDI #0757 2011/02/12



CMDI #0757 2011/02/12




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0096 C.
0097 C.
0098 C. *****
0099 C. OP/OGY1;4YEi;YAYOX
0100 C. *****
0101 C.
0102 C. ;aOP/OGY1;4YEi;a
0103 S. OP op-880:OP
0104 ( )
0105 S. OG og-880:OG
0106 ( )
0107 C.
0108 C. ;aNMOG&OPf^°eYAYOX;a
0109 C. NMOG(0x200000-0x207FFF;§ 32 kbyte)
0110 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0111 BC (20 00 7f 01 02)
0112 C.          çç[HK1_DMP_TOP_ADRS_1]          EQ      40
0113 C.          çç[HK1_DMP_TOP_ADRS_0]          EQ       0
0114 C.          çç[HK1_DMP_BLOCK_NUM]          EQ     127
0115 C.          çç[HK1_DMP_REPEAT_NUM]         EQ       0
0116 C.          çç[HK1_DMA_DMP_PIM]           EQ     DHU
0117 +. DC 01-22 DHU_MODE_CHNG
0118 BC (07 0b f8)
0119 C.          çç[HK1_PKT_FORM_NO]            EQ       7
0120 C.          çç[HK1_PKT_GEN_TIME]          EQ     0.25 s
0121 C.          çç[HK1_S_TLM_BIT_RATE]         EQ     32k
0122 C.          çç[HK1_X_TLM_BIT_RATE]         EQ       4M
0123 C.          çç[HK1_DMP_CHK_FLG]           EQ     EXEC
0124 C. YAYOXx½^i»oð³IÇ§
0125 C.          çç[HK1_DMP_CHK_FLG]           EQ     NON
0126 C. RAM ID=NMOGaf½E¹ç.ê²IOKoð³IÇ§
0127 C.
0128 C. NMOG(0x208000-0x20FFFF;§ 32 kbyte)
0129 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0130 BC (20 80 7f 01 02)
0131 C.          çç[HK1_DMP_TOP_ADRS_1]          EQ     41
0132 C.          çç[HK1_DMP_TOP_ADRS_0]          EQ       0
0133 C.          çç[HK1_DMP_BLOCK_NUM]          EQ     127
0134 C.          çç[HK1_DMP_REPEAT_NUM]         EQ       0
0135 C.          çç[HK1_DMA_DMP_PIM]           EQ     DHU
0136 +. DC 01-22 DHU_MODE_CHNG
0137 BC (07 0b f8)
0138 C.          çç[HK1_PKT_FORM_NO]            EQ       7
0139 C.          çç[HK1_PKT_GEN_TIME]          EQ     0.25 s
0140 C.          çç[HK1_S_TLM_BIT_RATE]         EQ     32k
0141 C.          çç[HK1_X_TLM_BIT_RATE]         EQ       4M
0142 C.          çç[HK1_DMP_CHK_FLG]           EQ     EXEC
0143 C. YAYOXx½^i»oð³IÇ§
0144 C.          çç[HK1_DMP_CHK_FLG]           EQ     NON
0145 C. RAM ID=NMOGaf½E¹ç.ê²IOKoð³IÇ§
0146 C.
0147 C. NMOG(0x210000-0x2100FF;§ 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)
0148 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0149 BC (21 00 41 01 02)
0150 C.          çç[HK1_DMP_TOP_ADRS_1]          EQ     42
0151 C.          çç[HK1_DMP_TOP_ADRS_0]          EQ       0
0152 C.          çç[HK1_DMP_BLOCK_NUM]          EQ     65
0153 C.          çç[HK1_DMP_REPEAT_NUM]         EQ       0
0154 C.          çç[HK1_DMA_DMP_PIM]           EQ     DHU
0155 +. DC 01-22 DHU_MODE_CHNG
0156 BC (07 0b f8)
0157 C.          çç[HK1_PKT_FORM_NO]            EQ       7
0158 C.          çç[HK1_PKT_GEN_TIME]          EQ     0.25 s
0159 C.          çç[HK1_S_TLM_BIT_RATE]         EQ     32k
0160 C.          çç[HK1_X_TLM_BIT_RATE]         EQ       4M
0161 C.          çç[HK1_DMP_CHK_FLG]           EQ     EXEC
0162 C. YAYOXx½^i»oð³IÇ§
0163 C.          çç[HK1_DMP_CHK_FLG]           EQ     NON
0164 C. RAM ID=NMOG, RAM ID=OPaf½E¹ç.ê²IOKoð³IÇ§
0165 C.
0166 C. ***** oE²¼oI½A´¶A°oEÉ¬oA÷¿@ (¼åµ-YAYOXx½e½çoðAÕAæoÇ¼^a¬oE¼i¹çoçoâ) *****
0167 C. DHUYâ;4YEi;E½Y½, Y1;4YEi;EoðIã¹
0168 +. DC 01-22 DHU_MODE_CHNG
0169 BC (02 0a f8)
0170 C.          çç[HK1_PKT_FORM_NO]            EQ       2
0171 C.          çç[HK1_PKT_GEN_TIME]          EQ     0.5S
0172 C.          çç[HK1_S_TLM_BIT_RATE]         EQ     32K
0173 C.          çç[HK1_X_TLM_BIT_RATE]         EQ       4M
0174 C.
0175 C. *****
0176 C. TI-CMD SET (OPOG STOP/COPY/START)
0177 C. *****
0178 C.
0179 C. NOTICE ;§ OPOG UPLOAD¬-Á÷¿@NGuI½i¹ç;ç°E²¼oI½TI-CMDÁ÷¿@aI½A¹Ôo.¬Eoð³oE;f
0180 C.          oEo¿;çSEToEDUMPaIÆ±°iYNY¹oç¹Ôo|o³oE;f
0181 C.
0182 C. TIY³YpYóYEoðAÐI¿(UT)
0183 +. TI 2011-02-08 10:05:00.0
0184 DC 01-B3 DHU_OP_STOP
0185 C.          çç[HK1_TI_CMD_NUM]            EQ     1COUNTUP
0186 C.
0187 +. TI 2011-02-08 10:05:01.0
0188 DC 01-B4 DHU_OP_COPY
0189 C.          çç[HK1_TI_CMD_NUM]            EQ     1COUNTUP
0190 C.
0191 +. TI 2011-02-08 10:05:01.0
0192 DC 01-B5 DHU_OPOG_COPY
0193 C.          çç[HK1_TI_CMD_NUM]            EQ     1COUNTUP

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0096 C.
0097 C.
0098 . C. ***** AOCs Commands (Tracking Curve Upload) *****
0099 C. Upload the Orbit Element and the Target Attitude
0100 C. RAM-ID:TARGET_ATT
0101 . S. RAM ram-150:TARGET_ATT
0102 ( )
0103 C.
0104 C.
0105 C. Set the dump memory area of TARGET_ATT
0106 +. DC 02-48 AOCU_DUMP_SET
0107 BC (07 00 00 00 18 00)
0108 C.
0109 C. <A_STS1>[MEMORY OPERATE STATUS] ADRS = 070000 [ ]
0110 C.
0111 C.
0112 C. Change the TLMFormatNo for the AOCs Dump Format
0113 +. DC 01-22 DHU_MODE_CHNG
0114 BC (04 0b f8)
0115 C.
0116 C. Wait for AOCSDUMP to end
0117 C.
0118 . C. Check the dump memory
0119 C.
0120 C. Result = OK [ ]
0121 C.
0122 +. DC 01-22 DHU_MODE_CHNG
0123 BC (02 0a f8)
0124 C.
0125 C. <A_***>[TLM STS] FMT = 2 [ ]
0126 C.
0127 +. DC 02-8E AOCU_ORB_UPD
0128 . C.
0129 . C. ***** AOCs Commands (Orbital Element Update) *****
0130 C. Update the orbital element
0131 +. DC 02-50 AOCU_ORB_PRPGT_START
0132 BC (16)
0133 +. DC 02-8E AOCU_ORB_UPD
0134 C.
0135 C. <A_ORB>[ORBIT] EPC = 3563113.2 +- 1.0 (s) [ ]
0136 C.
0137 . C.
0138 . C. Load OBSTBL, dump OBSTBL, enable EIS mode changes
0139 +. DC 07-FC EIS_MODE_MANU
0140 BC (21 02)
0141 . C. Verify EIS in MANUAL mode
0142 . C. Estimated OBSTBL upload time is 4s
0143 C. *****
0144 C. EIS START OBSTBL LOAD
0145 C. *****
0146 . S. RAM ram-820:EIS_OBSTBL
0147 ( )
0148 +. DC 07-FC EIS_DUMP_OBSTBL
0149 BC (07 07 07 00 00 70 00)
0150 C.
0151 C. Execute, after the success of OBSTBL upload.
0152 C. Set EIS TI-commands
0153 +. TI 2011-02-08 10:09:50.0
0154 DC 07-FC EIS_MODE_CHG_ENA
0155 BC (20)
0156 . C. [ ] [HK1_TI_CMD_NUM] EQ 1 COUNTUP
0157 C. *****
0158 C. EIS END OBSTBL LOAD
0159 C. *****
0160 C.
0161 . C. ***** MDP 'ûÄîâî»ö¼ÝðËÄð¹ñèDCBC·x²è *****
0162 C. (%â°îÝÔÝÄÝËÝÞÝËÝÑÝ¼ÝèñÈ¾¼ñ¼Ä»Û¹ñè)
0163 . S. DC-BC dcbc-402:DCBC
0164 (MDP_known_event)
0165 C.
0166 C.
0167 . C. ***** ÝÐÝ¹·Ï Daily±¿ÎÑèË'Ø¹ñèDCBC·x²è *****
0168 . S. DC-BC dcbc-153:DCBC
0169 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0170 C.
0171 C.
0172 . C. ;ãLOSÝÄÝ§ÝÄÝ¹¼Ä»Û;ã
0173 C.
0174 . C. ***** LOS *****
0175 C.
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(a) Spacecraft Operation Procedure (real-commands)

```
main-882 2011-02-08 11:07:28 149 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. ;ãAOSYÁY$YÁY-¼Á»Û;ä
0005 C.
0006 C. YÁYB;¼Y³YF¥ÖYÉÁ+¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCs : Reload orbital element (send every contact) *****
0010 C. Áí;È□¿□Á□•µ°È»Í×ÁÇ□íYçYÁY×Yí;¼YÉ;ÈÈèµ•ííÉ;È□È¼°Ç□□•□¿¼í¹ç□Í;çÁ®, ù□¹□è□□□çÁ+¿®□•□È□□□³□È;f
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 C.
0015 C. ***** XRT START *****
0016 C.
0017 +. DC 07-F0 MDP_XRT_CTRL_MANU
0018 BC (c1)
0019 + DC 07-F0 MDP_XRT_MODE_STBY
0020 BC (c3)
0021 . C. ----- Success Verify ? OK / NG ____
0022 C.
0023 C. XRT Obs. Table Upload
0024 . S. RAM ram-291:MDP_OBS_X
0025 ( )
0026 C.
0027 +. DC 07-F0 MDP_DUMP_XRTTBL
0028 BC (84 07 00 00 00 3a d4)
0029 . C. ----- Comparison Check ? OK / ERR ____
0030 C.
0031 C.
0032 +. DC 07-F0 MDP_XRT_ROI_SET
0033 BC (cd 01 b1 b1 04 04)
0034 + DC 07-F0 MDP_XRT_ROI_SET
0035 BC (cd 02 b1 b1 08 08)
0036 + DC 07-F0 MDP_XRT_ROI_SET
0037 BC (cd 03 b1 b1 08 08)
0038 + DC 07-F0 MDP_XRT_ROI_SET
0039 BC (cd 04 b1 b1 06 06)
0040 + DC 07-F0 MDP_XRT_ROI_SET
0041 BC (cd 05 85 83 06 06)
0042 + DC 07-F0 MDP_XRT_ROI_SET
0043 BC (cd 06 85 83 06 06)
0044 + DC 07-F0 MDP_XRT_ROI_SET
0045 BC (cd 07 80 80 06 08)
0046 + DC 07-F0 MDP_XRT_ROI_SET
0047 BC (cd 0f 80 80 06 06)
0048 + DC 07-F0 MDP_XRT_ROI_SET
0049 BC (cd 10 80 80 08 08)
0050 + DC 07-F0 MDP_XRT_FLD_ENA
0051 BC (d8)
0052 + DC 07-F0 MDP_XRT_FLRCTRL_ENA
0053 BC (c8)
0054 + DC 07-F0 MDP_XRT_ARS_DIS
0055 BC (d5)
0056 +. DC 07-F0 MDP_XRT_QT_PROG_SET
0057 BC (c4 0b)
0058 +. DC 07-F0 MDP_XRT_FL_PROG_SET
0059 BC (c5 10)
0060 . C. ----- Success Verify ? OK / NG ____
0061 C.
0062 C.
0063 . C. All OK? Yes--> Please Proceed. / No --> Stop here.
0064 C.
0065 +. DC 07-F0 MDP_XRT_MODE_OBSV
0066 BC (c2)
0067 +. DC 07-F0 MDP_XRT_CTRL_AUTO
0068 BC (c0)
0069 +. TI 2011-02-08 10:09:02.0
0070 DC 07-F0 MDP_XRT_MODE_OBSV
0071 BC (c2)
0072 +. TI 2011-02-08 10:09:04.0
0073 DC 07-F0 MDP_XRT_CTRL_AUTO
0074 BC (c0)
0075 . C. ----- Success Verify ? OK / NG ____
0076 C.
0077 C. ***** XRT END *****
0078 . C. *****
0079 C. SOT table upload
0080 C. *****
0081 . C. < Stop FG table >
0082 +. DC 07-F0 MDP_FG_CTRL_MANU
0083 BC (51)
0084 . C. -----
0085 C. MDP_FG_CTRL_MODE = MANU [ ]
0086 C. -----
0087 C.
0088 . C. <Upload FG Observation Table>
0089 . S. RAM ram-265:MDP_OBS_F
0090 ( )
0091 C.
0092 . C. < Dump RAMID=MDP_OBS_F >
0093 +. DC 07-F0 MDP_DUMP_FGTBL
0094 BC (82 07 00 00 00 38 b8)
0095 C. -----
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0096 C. MDP_OBS_F verify = OK/NG [ ]
0097 C. -----
0098 C.
0099 . C. < Upload DPL table >
0100 C.
0101 C. STS_CHK=OFF=
0102 C.
0103 . S. RAM ram-271:MDP_DPL
0104 ( )
0105 C.
0106 . C. < Dump RAMID=MDP_DPL >
0107 +. DC 07-F0 MDP_DUMP_FGTBL
0108 BC (82 07 00 38 b8 00 40)
0109 C. -----
0110 C. MDP_DPL verify = OK [ ]
0111 C. -----
0112 C.
0113 C. STS_CHK=ON=
0114 C.
0115 . C. < Update MDP DSC PAR1 >
0116 +. DC 07-F0 MDP_DSC_PAR1_UPDATE
0117 BC (4c)
0118 C. MDP_CMD_CODE = F04C0700[ ]
0119 C. MDP_CMD_CNT (count-up 1) [ ]
0120 C. -----
0121 C.
0122 . C.
0123 C. *****
0124 C. SOT TI command set
0125 C. *****
0126 C. Execute, after the success of TBL upload.
0127 +. TI 2011-02-08 10:09:18.0
0128 DC 07-F0 MDP_SOT_MODE_OBSV
0129 BC (40)
0130 . C. -----
0131 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0132 C. -----
0133 C.
0134 C.
0135 . C. ***** MDP ^úÃîï»ô¼ÝªËÄª¹ªèDCBC•x²è *****
0136 C. (¼ªºïÿÓÿÁÿÈÿÏÿÙÿáÿçÿèª¼ª¹ª»Ûª¹ªè)
0137 . S. DC-BC dcbc-402:DCBC
0138 (MDP_known_event)
0139 C.
0140 C.
0141 . C. ***** ÝDÿ¹•Ï Daily±¼ÏñªË¹ªèDCBC•x²è *****
0142 . S. DC-BC dcbc-153:DCBC
0143 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0144 C.
0145 C.
0146 . C. ;ãLOSÿÁÿÛÿÃÿ¹¼ª»Ûª¹ªä
0147 C.
0148 . C. ***** LOS *****
0149 C.

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*** OP Sequence for XRT ***

2011/02/08	10:19:54.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	10:19:56.0	XRT_FOCUS_RECALIBRATE_432_OG [0x1b0]			
		XRT_FOCUS_RECAL	2	07-F8	78 00
2011/02/08	10:20:00.0	AOCS_Ore-point_Start_1_OG [0x097]			
		AOCU_NM	5	02-76	01 00 00 00 00
2011/02/08	10:23:56.0	XRT_FOCUS_POSITION_409_OG [0x199]			
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2011/02/08	10:24:16.0	XRT_FLD_ENA_411_OG [0x19b]			
		MDP_XRT_FLD_ENA	1	07-F0	d8
2011/02/08	10:24:18.0	XRT_FLRCTRL_ENA_413_OG [0x19d]			
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2011/02/08	10:24:20.0	XRT_AEC_RESET_443_OG [0x1bb]			
		MDP_XRT_AEC_RESET	1	07-F0	d0
2011/02/08	10:24:22.0	XRT_ARS_DIS_437_OG [0x1b5]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2011/02/08	10:26:54.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	10:26:56.0	XRT_QT_PROG_SET_425_OG [0x1a9]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0a
2011/02/08	10:26:58.0	XRT_FL_PROG_SET_421_OG [0x1a5]			
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 10
2011/02/08	10:27:00.0	XRT_CTRL_AUTO_406_OG [0x196]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	15:30:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	15:30:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	15:30:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	15:33:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	15:44:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	15:45:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	15:45:30.5	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	15:45:32.5	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	15:45:34.5	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	15:48:44.5	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	15:53:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	15:54:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	17:06:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	17:06:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	17:06:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	17:09:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	17:30:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	17:31:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	18:43:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	18:43:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	18:43:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	18:46:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	19:07:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	19:08:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	20:21:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	20:21:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	20:21:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	20:24:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	20:44:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	20:45:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	21:58:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/08	21:58:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	21:58:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	22:01:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	22:20:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/08	22:21:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/08	23:36:00.0	XRT_CTRL_MANU_408_OG [0x198]			

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2011/02/08	23:36:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_CTRL_MANU	1	07-F0	c1
			MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/08	23:36:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/08	23:39:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/08	23:48:00.0	XRT_Custom_418_OG [0x1a2]				
2011/02/08	23:49:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	01:03:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	01:03:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	01:03:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	01:06:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	01:19:00.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	01:20:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	02:35:00.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	02:35:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	02:35:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	02:38:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	02:55:30.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	02:56:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	04:03:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	04:03:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	04:03:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	04:06:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	04:33:00.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	04:34:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	05:44:00.5	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	05:44:02.5	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	05:44:04.5	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	05:47:14.5	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	06:10:30.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	06:11:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	07:24:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	07:24:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	07:24:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	07:27:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	07:47:30.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	07:48:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	09:04:00.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	09:04:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	09:04:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	09:07:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	09:23:30.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	09:24:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	10:46:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	10:46:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	10:46:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	10:49:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	10:50:00.0	XRT_Custom_418_OG [0x1a2]				
2011/02/09	10:51:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]				
			MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	14:32:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	14:32:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	14:32:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8

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2011/02/09	14:35:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	14:42:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	14:43:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	16:06:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	16:06:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	16:06:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	16:09:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	16:30:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	16:31:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	17:43:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	17:43:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	17:43:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	17:46:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	18:07:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	18:08:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	19:20:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	19:20:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	19:20:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	19:23:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	19:43:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	19:44:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	20:58:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	20:58:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	20:58:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	21:01:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	21:21:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	21:22:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/09	22:35:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/09	22:35:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/09	22:35:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/09	22:38:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/09	22:56:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/09	22:57:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	00:12:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	00:12:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	00:12:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	00:15:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	00:21:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	00:22:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	01:36:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	01:36:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	01:36:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	01:39:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	01:55:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	01:56:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	03:11:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	03:11:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	03:11:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	03:14:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	03:32:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	03:33:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0

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2011/02/10	04:41:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	04:41:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	04:41:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	04:44:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	05:10:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	05:11:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	06:22:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	06:22:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	06:22:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	06:25:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	06:47:30.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	06:48:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	08:02:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	08:02:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/02/10	08:02:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/02/10	08:05:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/02/10	08:24:00.0	XRT_Custom_418_OG [0x1a2]			
2011/02/10	08:25:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/02/10	09:43:54.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/02/10	09:44:00.0	AOCS_ORe-point_Start_2_OG [0x098]			
		AOCU_NM	5	02-76	00 00 00 00 00