

Period: 2011/10/29 10:51:00 - 2011/11/03 10:07:00

XOB #18AD: Synoptic Q95 2x2 - Al/mesh(16/1024) + Dark cal(2x2 4x4 8x8 512 Q98) + Dark cal(1x1 512x2048 -1x1 2048x512) + Ti-poly(33/2048) + Thin-Be(12/2048)																
Term		Pointing (x, y)						Comment								
10/31 18:03:00 - 10/31 18:09:54		Fixed (0.0, 0.0)						synoptic								
11/01 06:19:30 - 11/01 06:26:24		Fixed (0.0, 0.0)						synoptic, shifted 16.5 min								
PROG= 04																
└ Subr= 1																
1-time(s)		12.0sec														
Seqn= 7		1-time(s) 4.0sec														
└ Open/Al-mesh		Open/Al-mesh	close	Safe	Norm	16ms	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
└ Open/Al-mesh		Open/Al-mesh	close	Safe	Norm	1.00s	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
Seqn= 5		1-time(s) 2.0sec														
└ Open/Ti-poly		Open/thick-Al	close	Safe	Dark	500ms	Obs	2x2	2048x2048 (1024, 1024)	Q=98	0	0	2.0sec			
└ Open/Ti-poly		Open/thick-Al	close	Safe	Dark	500ms	Obs	4x4	2048x2048 (1024, 1024)	Q=98	0	0	2.0sec			
└ Open/Ti-poly		Open/thick-Al	close	Safe	Dark	500ms	Obs	8x8	2048x2048 (1024, 1024)	Q=98	0	0	2.0sec			
└ Open/Ti-poly		Open/thick-Al	close	Safe	Dark	500ms	Obs	1x1	2048x512 (1024, 1024)	DPCM	0	0	2.0sec			
└ Open/Ti-poly		Open/thick-Al	close	Safe	Dark	500ms	Obs	1x1	512x2048 (1024, 1024)	DPCM	0	0	2.0sec			
Seqn= 8		1-time(s) 4.0sec														
└ Open/Ti-poly		Open/Ti-poly	close	Safe	Norm	32ms	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
└ Open/Ti-poly		Open/Ti-poly	close	Safe	Norm	2.00s	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
Seqn= 75		1-time(s) 2.0sec														
└ thin-Be/Open		thin-Be/Open	close	Safe	Norm	125ms	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
└ thin-Be/Open		thin-Be/Open	close	Safe	Norm	2.83s	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
Seqn= 4		1-time(s) 2.0sec														
└ Open/G-band		Open/G-band	open	Safe	Norm	16ms	Obs	2x2	2048x2048 (1024, 1024)	Q=95	0	0	2.0sec			
Default Filter		Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)	Comp.	AEC	Buffer	Interval			

XOB #1869: Flare standard obs. multifilter (thin-Be,med-Al,thick-Be 384x384 - Al-poly 512x512 2x2)		
Term	Pointing (x, y)	Comment
1	1	
2	2	
3	3	
4	4	
5	5	
6	6	
7	7	
8	8	
9	9	
10	10	
11	11	
12	12	
13	13	
14	14	
15	15	
16	16	
17	17	
18	18	
19	19	
20	20	
21	21	
22	22	
23	23	
24	24	
25	25	
26	26	
27	27	
28	28	
29	29	
30	30	
31	31	
32	32	
33	33	
34	34	
35	35	
36	36	
37	37	
38	38	
39	39	
40	40	
41	41	
42	42	
43	43	
44	44	
45	45	
46	46	
47	47	
48	48	
49	49	
50	50	
51	51	
52	52	
53	53	
54	54	
55	55	
56	56	
57	57	
58	58	
59	59	
60	60	
61	61	
62	62	
63	63	
64	64	
65	65	
66	66	
67	67	
68	68	
69	69	
70	70	
71	71	
72	72	
73	73	
74	74	
75	75	
76	76	
77	77	
78	78	
79	79	
80	80	
81	81	
82	82	
83	83	
84	84	
85	85	
86	86	
87	87	
88	88	
89	89	
90	90	
91	91	
92	92	
93	93	
94	94	
95	95	
96	96	
97	97	
98	98	
99	99	
100	100	

10/31 09:29:00 - 10/31 13:56:54 Track (671.3, 31.9) @ 10/31 06:08:30 # AR 11330 (HOP-202 officially 14-18UT).
10/31 14:00:00 - 10/31 17:59:54 Track (671.3, 31.9) @ 10/31 06:08:30 # AR 11330 (HOP-202 officially 14-18UT).
10/31 18:13:00 - 10/31 23:09:54 Fixed (-939.0, -190.0) # AR on the East Limb.
10/31 23:13:00 - 11/01 05:40:00 Track (775.8, 42.0) @ 10/31 23:10:00 # AR 11330.
11/01 06:29:30 - 11/01 08:45:00 Track (814.1, 46.6) @ 11/01 06:26:30 # AR 11330.

PROG= 13													1-time(s)			
Subr= 1		4-time(s)				2.0sec										
Seqn= 55		45-time(s)				20.0sec										
thin-Be/Open		med-Be/Open		close	Safe	Norm	250ms	Obs	1x1	384x384 (1024, 1024)		Q=95	3	0	2.0sec	
med-Al/Open		med-Al/thick-Al		close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)		Q=95	3	0	2.0sec	
Open/thick-Be		Open/thick-Be		close	Safe	Norm	2.00s	Obs	1x1	384x384 (1024, 1024)		Q=95	3	0	2.0sec	
Al-poly/Open		Al-poly/thick-Al		close	Safe	Norm	125ms	Obs	2x2	512x512 (1024, 1024)		Q=95	2	0	2.0sec	
Seqn= 90		1-time(s)				2.0sec										
Open/G-band		Open/G-band		open	Safe	Norm	63ms	Obs	1x1	384x384 (1024, 1024)		Q=98	0	0	2.0sec	
Open/thick-Al		Open/thick-Al		close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)		Q=98	0	0	2.0sec	
Open/thick-Al		Open/thick-Al		close	Safe	Dark	1.00s	Obs	2x2	512x512 (1024, 1024)		Q=98	0	0	2.0sec	
Subr= 2		1-time(s)				600.0sec										
Seqn= 89		1-time(s)				2.0sec										
Open/Al-mesh		Open/thick-Al		close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)		Q=95	1	0	2.0sec	
Open/Ti-poly		Open/thick-Be		close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)		Q=95	1	0	2.0sec	
Open/G-band		Open/G-band		open	Safe	Norm	63ms	Obs	1x1	384x384 (1024, 1024)		Q=98	0	0	2.0sec	
Open/Al-mesh		Open/Al-mesh		close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)		Q=98	0	0	2.0sec	
Default Filter		Thicker Filter		VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)		Comp.	AEC Buffer	Interval		

* * * * *

Active Region Search

* * * * *

NOT USED

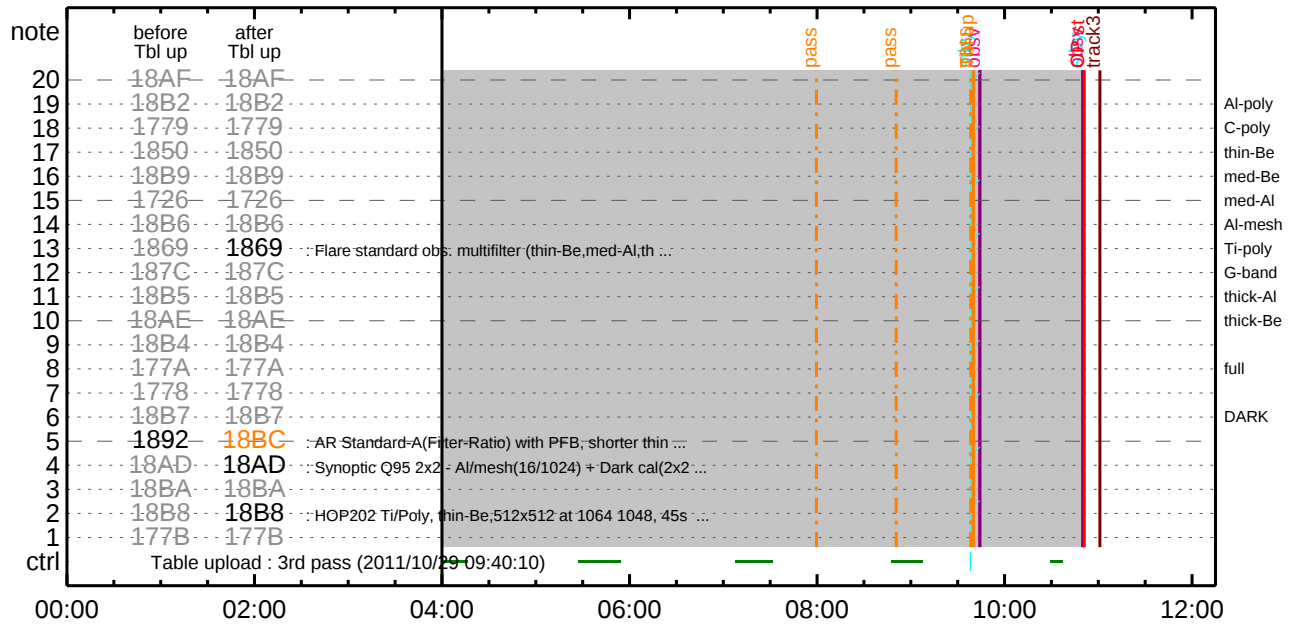
* * * * *

Flare Detection

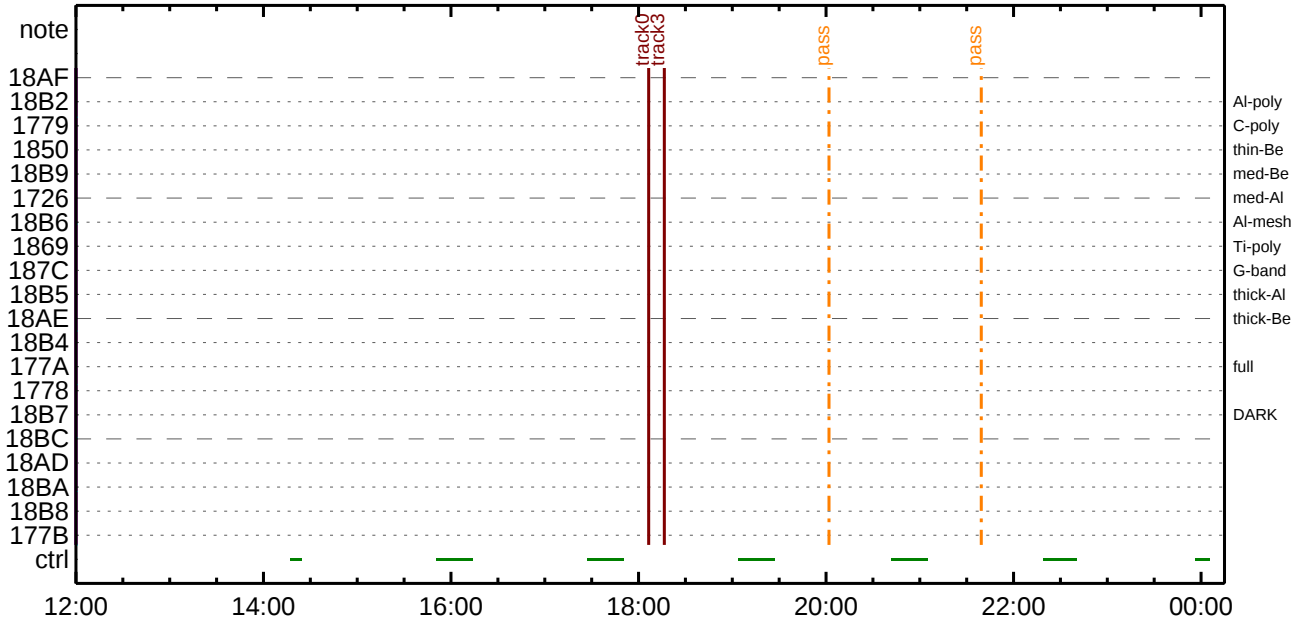
* * * * *

FLD Patrol												
Term			Pointing (x, y)						Comment			
10/31 18:10:16 - 11/01 06:16:46			Fixed (-939.0, -190.0)						# AR on the East Limb.			
11/01 06:26:46 - 11/03 10:07:00			Track (814.1, 46.6) @ 11/01 06:26:30						# AR 11330.			
Open/Ti-poly		Open/thick-Al		close	Safe	Norm	8ms	Obs	8x8	Q=50		30sec
Default Filter		Thicker Filter		VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)		Comp. AEC Buffer Interval

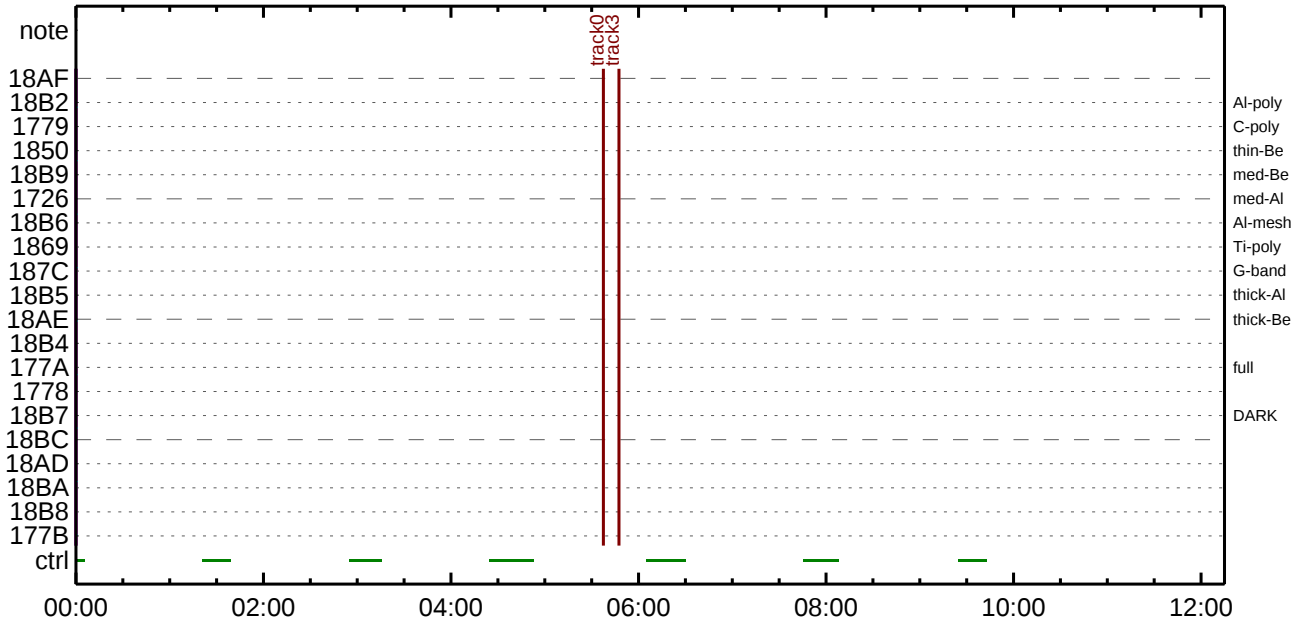
CMDI #0236 2011/10/29



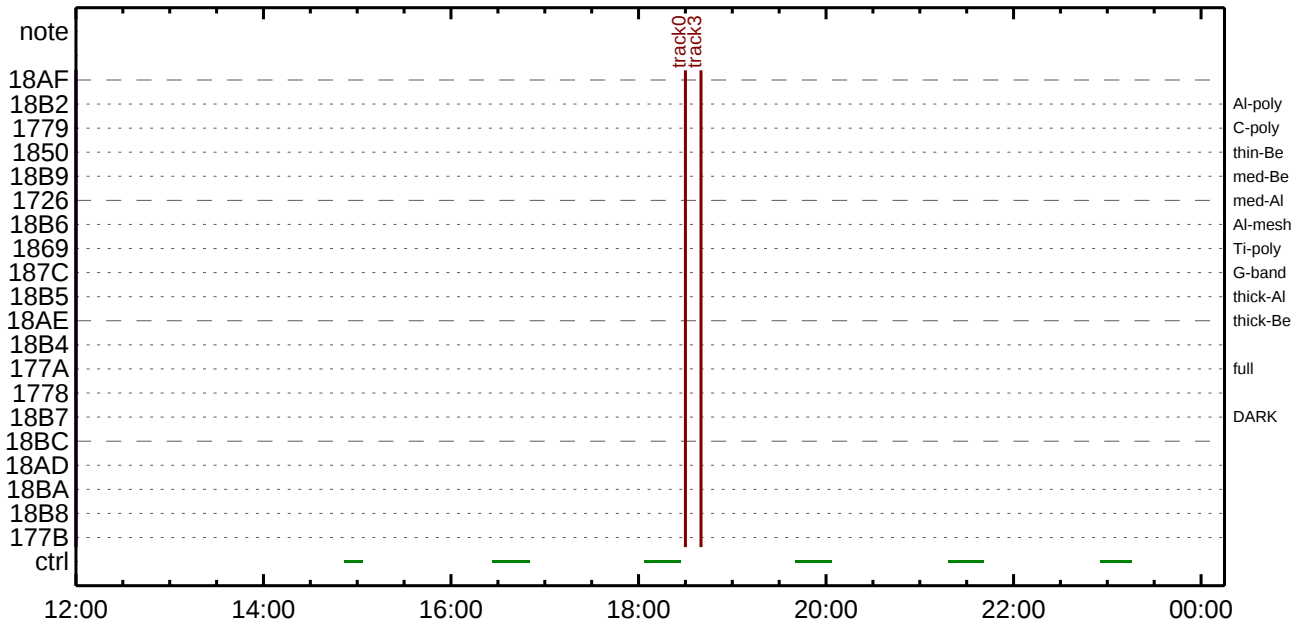
CMDI #0236 2011/10/29



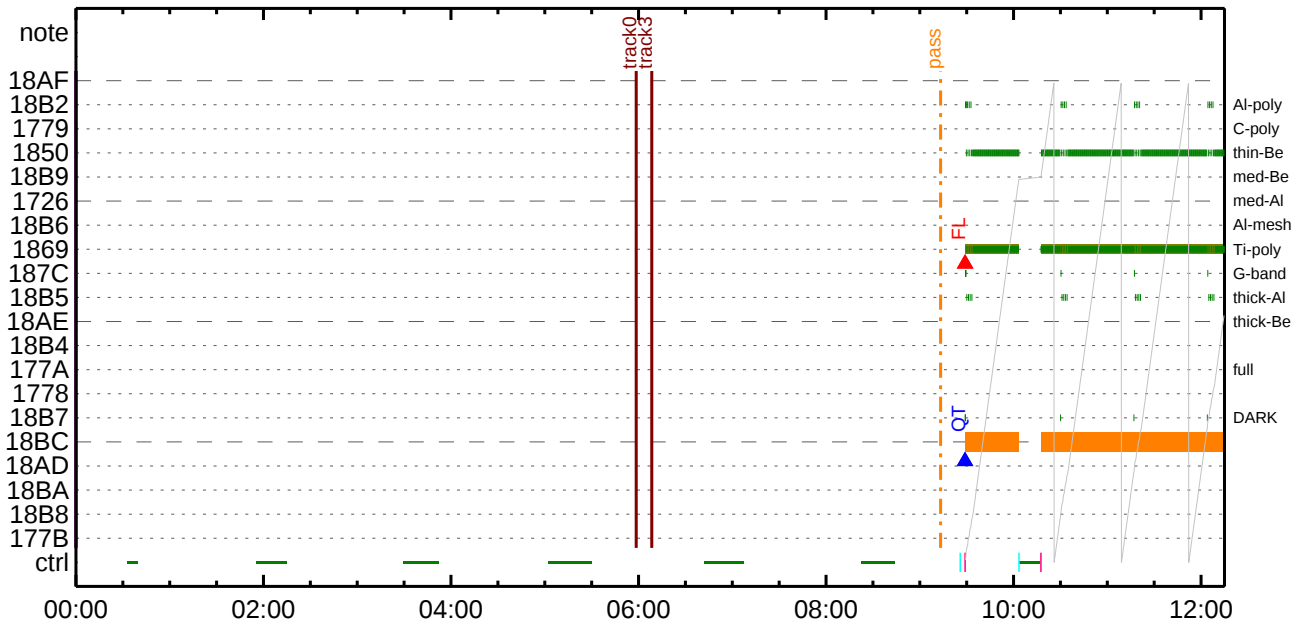
CMDI #0236 2011/10/30



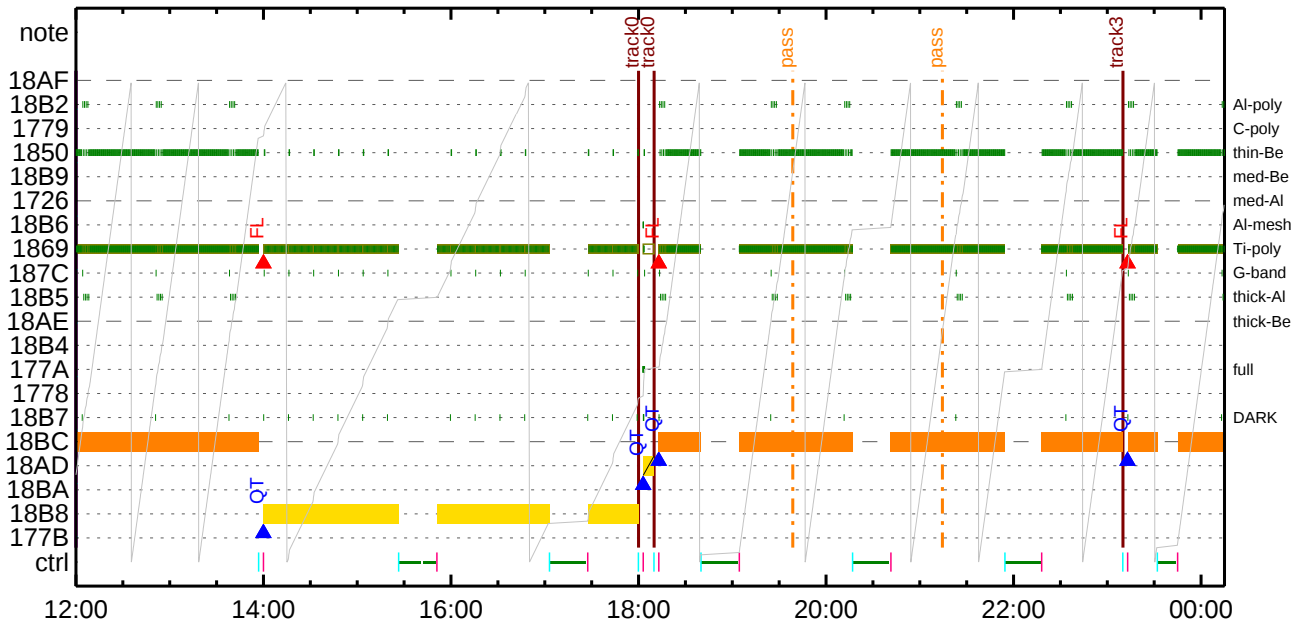
CMDI #0236 2011/10/30



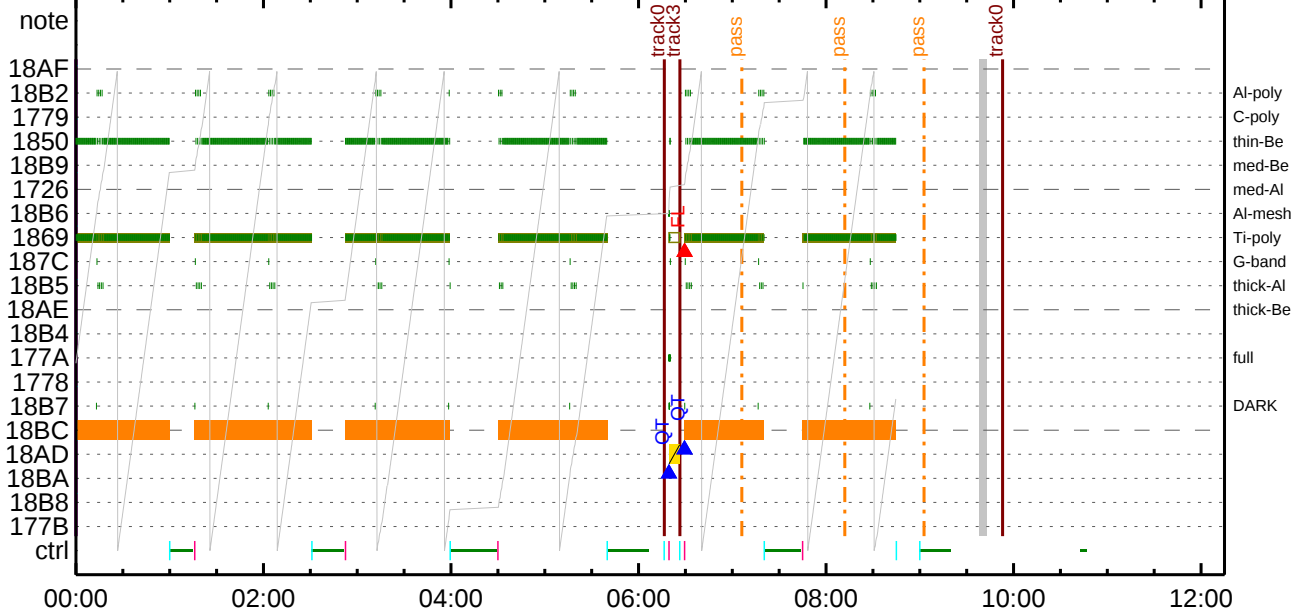
CMDI #0236 2011/10/31



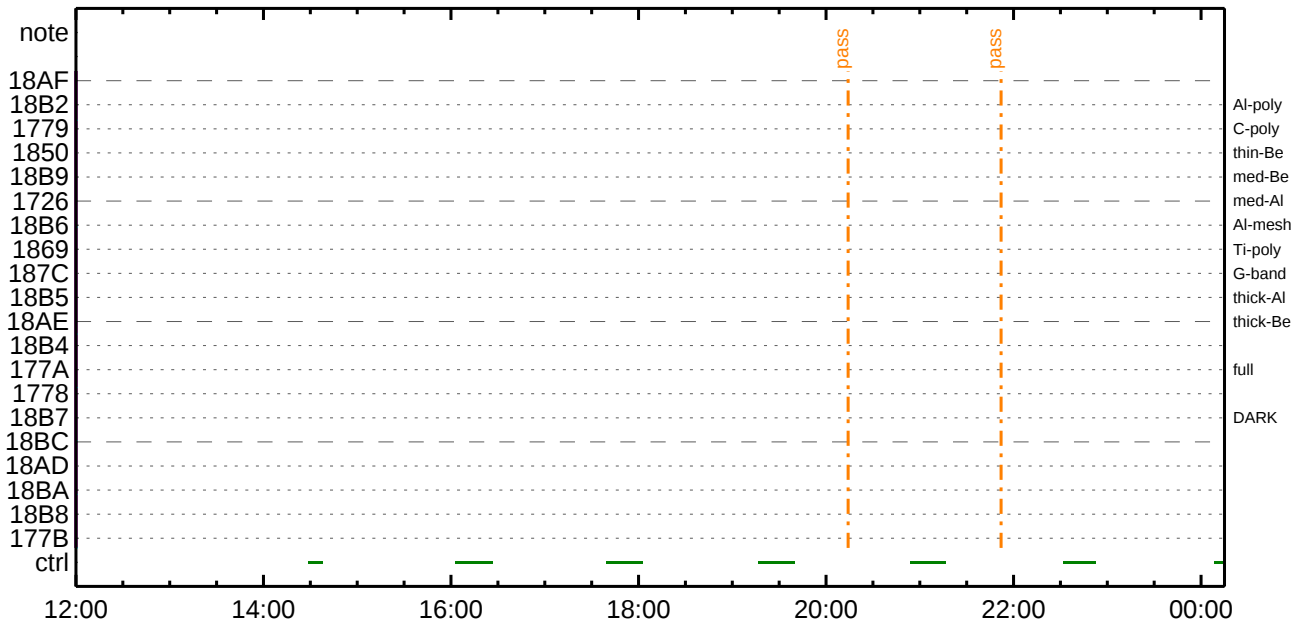
CMDI #0236 2011/10/31



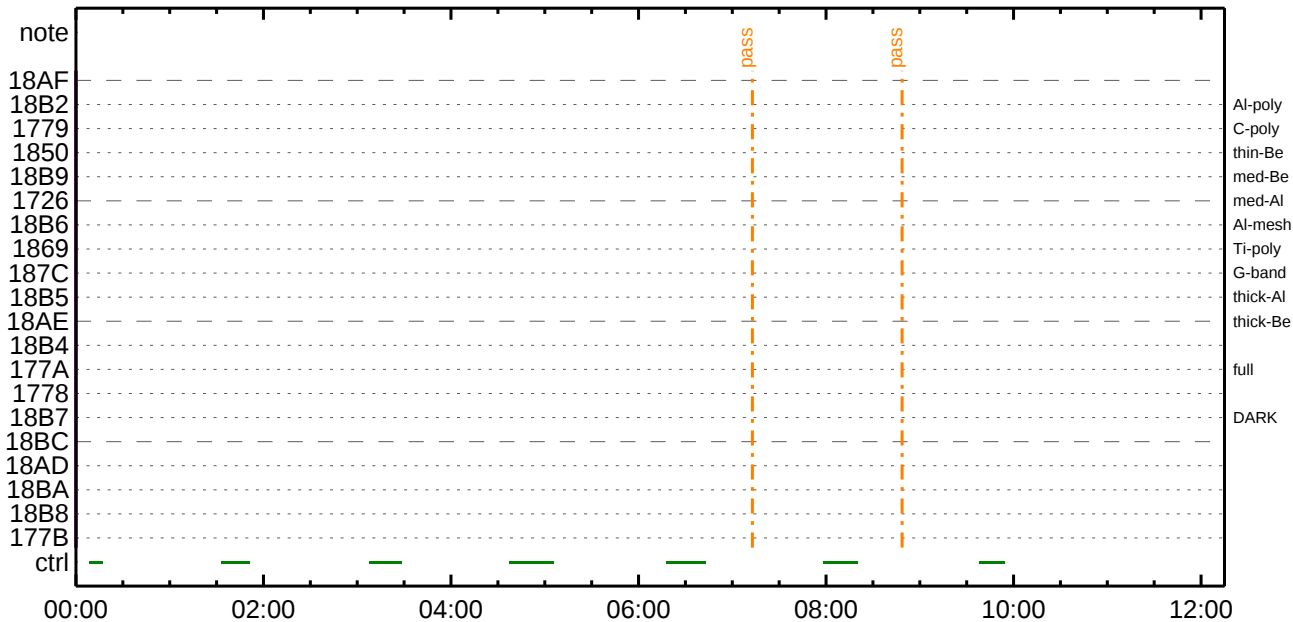
CMDI #0236 2011/11/01



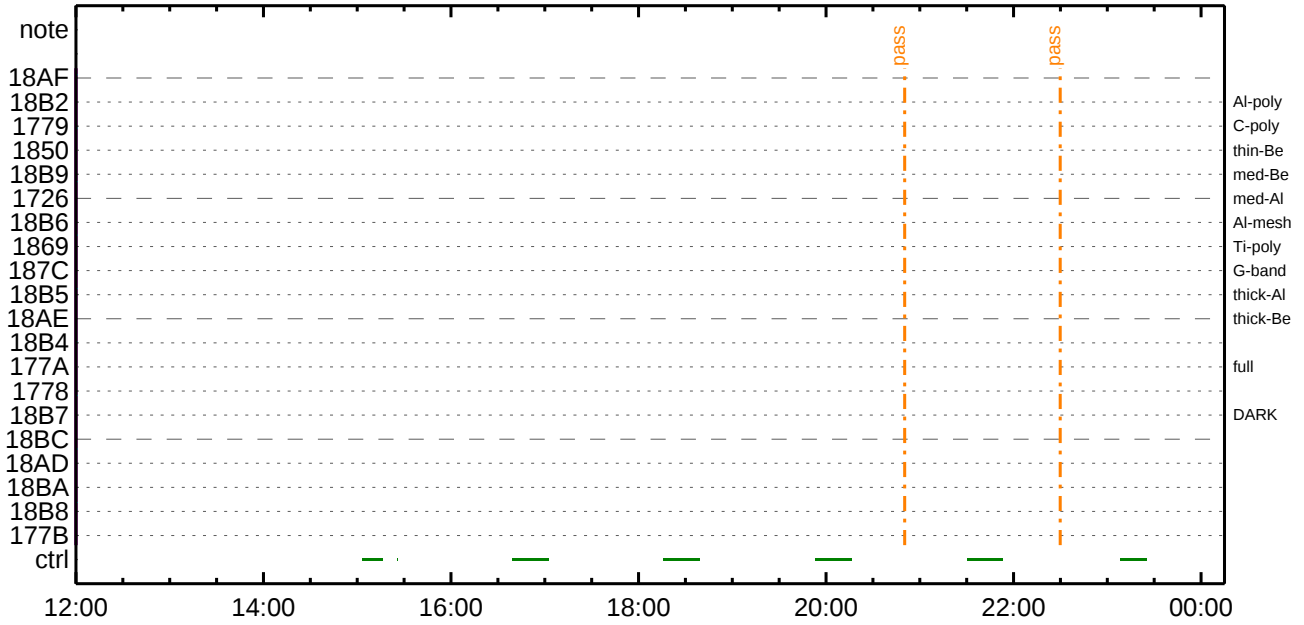
CMDI #0236 2011/11/01



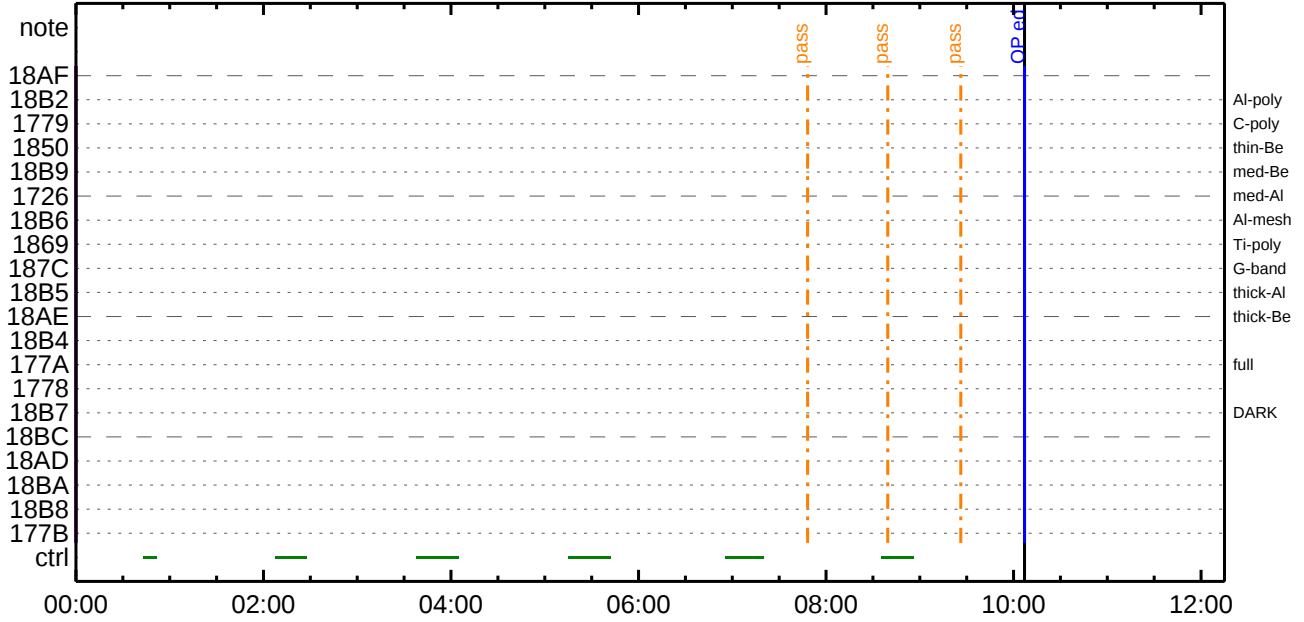
CMDI #0236 2011/11/02



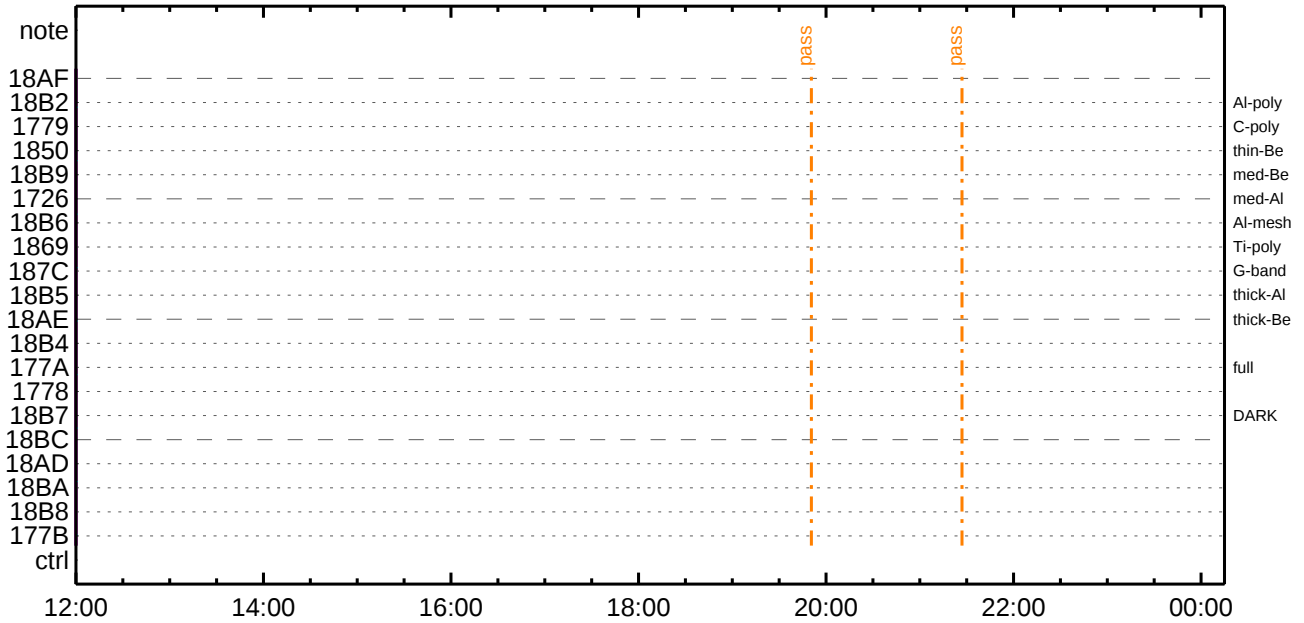
CMDI #0236 2011/11/02



CMDI #0236 2011/11/03



CMDI #0236 2011/11/03



```
main-427 2011-10-29 12:42:08 289 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. iãAOS¥Á¥$¥Ã¥¬¼Ä»Üjã
0005 C.
0006 C. ¥Ä¥ßj¼¥³¥Ð¥Ó¥ÉÄ÷¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCS : Reload orbital element (send every contact) *****
0010 C. Äi j Ê¤¿¤Ä¤•µ°Æ»I×AÇ¤I¥¢¥Ä¥×¥i j¼¥ÊjÊÊê½µ•îÊjÊ¤Ê¼°Ç¤¤•¤¿¼¹Ç¤I j ÇÄ®, ù¤¹¤è¤¤¤ÇÄ÷¿®¤¤•¤Ê¤¤¤³¤Èj£
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 . C. *****
0015 C. XÄ÷¿®µjON
0016 C. *****
0017 C. ¨ °ÆÄ, I×ÊÝ¤äLOS¤¤¤Ç¤I»p´Ö¤ò¹îî, ¤•jÇÊÔI×¤EXÄÓON¤I¹Ö¤Ê¤i¤Ê¤¤¤³¤Èj£
0018 C.
0019 +. DC 03-B4 TCIA_XPA_ON/HI
0020 M. WAIT_SEC 1
0021 + DC 03-84 TCIA_XMOD_ON
0022 M. WAIT_SEC 1
0023 + DC 03-95 TCIA_XMOD_QPSK
0024 C. ¢¢[HK1_XPA_ON/OFF] EQ ON
0025 C. ¢¢[HK1_XPA_PWR_HI/L0] EQ HI
0026 C. ¢¢[HK1_XMOD_ON/OFF] EQ ON
0027 C. ¢¢[HK1_XMOD_QPSK/PM] EQ QPSK
0028 C.
0029 . C. X¥Ð¥Ó¥É¥i¥Ä¥¬¼ÖÄÖ¤¬¼Äê¤¤•¤¿¤¤Èj¢°Ê²¼¤¤I°ÆÄ, ¼ê½Ç¤¤ò¼Ä¹Ö¤¤¹¤èj£
0030 C.
0031 . C. *****
0032 C. DR PT1 ÄI¾i°ÆÄ
0033 C. *****
0034 C. ¨ RESTARTjÊPT1jÊ¤¤•¤¿¤¤¼¹Ç¤I j¢°Ê²¼¤¤I¼Ä¹Ö¤¤¤¤i¢DCBC-150¤Ø¿Ê¤¤àj£
0035 C.
0036 . C. iãPT1°ÆÄ, ³«»Ijã
0037 +. DC 01-29 DHU_S/X_VC4_OFF
0038 + DC 06-C8 DR_PT1_REP_SEL
0039 BC (01 00)
0040 + DC 06-B3 DR_REP_START
0041 + DC 01-32 DHU_X_VC4_ON
0042 C. ¢¢[HK1_REP_PT_1/2] EQ PT1 (¼Ä¹Ö, j¼Ú)
0043 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¼Ú)
0044 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¼Ú)
0045 C.
0046 . C. iã¥¢¥ó¥Æ¥ÊÄÜÄØjÊÄ•Äº²ÖÊòjÊ, ä¤I°ÆÄ, °Æ³«jã
0047 +. DC 06-B3 DR_REP_START
0048 + DC 01-32 DHU_X_VC4_ON
0049 C. ¢¢[HK1_REP_PT_1/2] EQ PT1 (¼Ä¹Ö, j¼Ú)
0050 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¼Ú)
0051 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¼Ú)
0052 C.
0053 C.
0054 . C. PT1°ÆÄ, ¤¬¼«Æ°Ää»ß¤¤•¤¿, äj¢°Ê²¼¤¤ò¼Ä¹Ö¤¤¹¤èj£
0055 C. ¥¢¥ó¥Æ¥ÊÄÜÄØ¤¤ÄÄ•Äº²ÖÊò¤¬¼á¤¤¼¹Ç¤I ´Î»¤¤¹¤è¤¤¤¤ÇÄÖ¤Äj£
0056 C.
0057 . C. *****
0058 C. DR PT2 ÄI¾i°ÆÄ
0059 C. *****
0060 C. ¨ RESTARTjÊPT2jÊ¤¤•¤¿¤¤¼¹Ç¤I j¢°Ê²¼¤¤I¼Ä¹Ö¤¤¤¤i¢DCBC-151¤Ø¿Ê¤¤àj£
0061 C.
0062 . C. iãPT2°ÆÄ, ³«»Ijã
0063 +. DC 01-29 DHU_S/X_VC4_OFF
0064 + DC 06-C8 DR_PT2_REP_SEL
0065 BC (02 00)
0066 + DC 06-B3 DR_REP_START
0067 + DC 01-32 DHU_X_VC4_ON
0068 C. ¢¢[HK1_REP_PT_1/2] EQ PT2 (¼Ä¹Ö, j¼Ú)
0069 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¼Ú)
0070 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¼Ú)
0071 C.
0072 . C. iã¥¢¥ó¥Æ¥ÊÄÜÄØjÊÄ•Äº²ÖÊòjÊ, ä¤I°ÆÄ, °Æ³«jã
0073 +. DC 06-B3 DR_REP_START
0074 + DC 01-32 DHU_X_VC4_ON
0075 C. ¢¢[HK1_REP_PT_1/2] EQ PT2 (¼Ä¹Ö, j¼Ú)
0076 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¼Ú)
0077 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¼Ú)
0078 C.
0079 . C. *****
0080 C. DR°ÆÄ, Ää»ßj¢XÄ÷¿®µjOFF
0081 C. *****
0082 C.
0083 . C. iãDR°ÆÄ, Ää»ßjã
0084 +. DC 06-B4 DR_REP_STOP
0085 + DC 01-29 DHU_S/X_VC4_OFF
0086 C. ¢¢[HK1_REP_STA/STP] EQ STOP
0087 C. ¢¢[HK1_S_VC4_ON/OFF] EQ OFF
0088 C. ¢¢[HK1_X_VC4_ON/OFF] EQ OFF
0089 C.
0090 . C. iãXÄ÷¿®µjOFFjã
0091 +. DC 03-85 TCIA_XMOD_OFF
0092 M. WAIT_SEC 1
0093 + DC 03-B5 TCIA_XPA_OFF
0094 C. ¢¢[HK1_XMOD_ON/OFF] EQ OFF
0095 C. ¢¢[HK1_XPA_ON/OFF] EQ OFF
```

```
0096 . C.  
0097 . C.  
0098 . C. *****  
0099 . C. OP/OG¥¡ï¼¥É;| ¥À¥ó×  
0100 . C. *****  
0101 . C.  
0102 . C. ¡ãOP/OG¥¡ï¼¥É;ä  
0103 . S. OP      op-427:OP  
0104 . (  
0105 . S. OG      og-427:OG  
0106 . )  
0107 . C.  
0108 . C. ¡ãNMOG&OPÎî°è¥À¥ó×;jä  
0109 . C. NMOG(0x200000-0x207FFF;$ 32 kbyte)  
+ DC 01-23 DHU_DMA_DMP_PRM_SET  
0111 BC      (20 00 7f 01 02)  
0112 . C.                  ¢¢[HK1_DMP_TOP_ADRS_1]          EQ        40  
0113 . C.                  ¢¢[HK1_DMP_TOP_ADRS_0]          EQ         0  
0114 . C.                  ¢¢[HK1_DMP_BLOCK_NUM]           EQ       127  
0115 . C.                  ¢¢[HK1_DMP_REPEAT_NUM]           EQ         0  
0116 . C.                  ¢¢[HK1_DMA_DMP_PIM]              EQ       DHU  
+ DC 01-22 DHU_MODE_CHNG  
0117 BC      (07 0b f8)  
0118 . C.  
0119 . C.                  ¢¢[HK1_PKT_FORM_NO]             EQ         7  
0120 . C.                  ¢¢[HK1_PKT_GEN_TIME]            EQ     0.25 s  
0121 . C.                  ¢¢[HK1_S_TLM_BIT_RATE]           EQ       32k  
0122 . C.                  ¢¢[HK1_X_TLM_BIT_RATE]           EQ        4M  
0123 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     EXEC  
0124 . C. ¥À¥ó×½ª¹»ð³İÇŞ  
0125 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     NON  
0126 . C. RAM ID=NMOG¤¹Ê¹Ç•ë²İOK¤ò³İÇŞ  
0127 . C.  
0128 . C. NMOG(0x208000-0x20FFFF;$ 32 kbyte)  
+ DC 01-23 DHU_DMA_DMP_PRM_SET  
0130 BC      (20 80 7f 01 02)  
0131 . C.                  ¢¢[HK1_DMP_TOP_ADRS_1]          EQ        41  
0132 . C.                  ¢¢[HK1_DMP_TOP_ADRS_0]          EQ         0  
0133 . C.                  ¢¢[HK1_DMP_BLOCK_NUM]           EQ       127  
0134 . C.                  ¢¢[HK1_DMP_REPEAT_NUM]           EQ         0  
0135 . C.                  ¢¢[HK1_DMA_DMP_PIM]              EQ       DHU  
+ DC 01-22 DHU_MODE_CHNG  
0137 BC      (07 0b f8)  
0138 . C.  
0139 . C.                  ¢¢[HK1_PKT_FORM_NO]             EQ         7  
0140 . C.                  ¢¢[HK1_PKT_GEN_TIME]            EQ     0.25 s  
0141 . C.                  ¢¢[HK1_S_TLM_BIT_RATE]           EQ       32k  
0142 . C.                  ¢¢[HK1_X_TLM_BIT_RATE]           EQ        4M  
0143 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     EXEC  
0144 . C. ¥À¥ó×½ª¹»ð³İÇŞ  
0145 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     NON  
0146 . C. RAM ID=NMOG¤¹Ê¹Ç•ë²İOK¤ò³İÇŞ  
0147 . C.  
0148 + DC 01-23 DHU_DMA_DMP_PRM_SET  
0149 BC      (21 00 41 01 02) 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)  
0150 . C.                  ¢¢[HK1_DMP_TOP_ADRS_1]          EQ        42  
0151 . C.                  ¢¢[HK1_DMP_TOP_ADRS_0]          EQ         0  
0152 . C.                  ¢¢[HK1_DMP_BLOCK_NUM]           EQ       65  
0153 . C.                  ¢¢[HK1_DMP_REPEAT_NUM]           EQ         0  
0154 . C.                  ¢¢[HK1_DMA_DMP_PIM]              EQ       DHU  
+ DC 01-22 DHU_MODE_CHNG  
0155 BC      (07 0b f8)  
0156 . C.  
0157 . C.                  ¢¢[HK1_PKT_FORM_NO]             EQ         7  
0158 . C.                  ¢¢[HK1_PKT_GEN_TIME]            EQ     0.25 s  
0159 . C.                  ¢¢[HK1_S_TLM_BIT_RATE]           EQ       32k  
0160 . C.                  ¢¢[HK1_X_TLM_BIT_RATE]           EQ        4M  
0161 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     EXEC  
0162 . C. ¥À¥ó×½ª¹»ð³İÇŞ  
0163 . C.                  ¢¢[HK1_DMP_CHK_FLG]             EQ     NON  
0164 . C. RAM ID=NMOG,RAM ID=OP¤¹Ê¹Ç•ë²İOK¤ò³İÇŞ  
0165 . C.  
0166 . C. **** °È²¼¤¹%Ä´¶Á°¤ĖĖ-¤ºÁ÷Ł® (%âµ-¥À¥ó×¾ē½Ç¤òÃŒæ¤Ç½¤¤¨¤ě%ı¹Ç¤Ç¤â) ****  
0167 . C. DHU¥â;¼¥É;Ė¼Y½. ¥ł;¼¥ĖjĖ¤òİā¤¹  
+ DC 01-22 DHU_MODE_CHNG  
0169 BC      (02 0a f8)  
0170 . C.                  ¢¢[HK1_PKT_FORM_NO]             EQ         2  
0171 . C.                  ¢¢[HK1_PKT_GEN_TIME]            EQ     0.5S  
0172 . C.                  ¢¢[HK1_S_TLM_BIT_RATE]           EQ       32K  
0173 . C.                  ¢¢[HK1_X_TLM_BIT_RATE]           EQ        4M  
0174 . C.  
0175 . C. *****  
0176 . C. TI-CMD SET (OPOG STOP/COPY/START)  
0177 . C. *****  
0178 . C.  
0179 . C. NOTICE i$ OPOG UPLOAD¤-Á÷ŁNG¤¹İ¹Çj¢°È²¼¤¹TI-CMDÁ÷Ł®¤¹¼Å¹Ô¤•¤Ė¤¤¤³¤Ėj£  
0180 . C. ¤¤¤Łj¢SET¤ĖDUMP¤İÆ±°ıİN¥¹çÇ¹Ô¤ı³¤Ėj£  
0181 . C.  
0182 . C. Tİ¥³¥¤¥ó¥É¤òÂĐİŁ(UT)  
+ TI 2011-10-29 10:46:00.0  
0184 DC 01-B3 DHU_OP_STOP  
0185 . C.                  ¢¢[HK1_TI_CMD_NUM]                EQ    1COUNTUP  
0186 . C.  
+ TI 2011-10-29 10:46:01.0  
0188 DC 01-B4 DHU_OP_COPY  
0189 . C.                  ¢¢[HK1_TI_CMD_NUM]                EQ    1COUNTUP  
0190 . C.  
0191 + TI 2011-10-29 10:46:01.0  
0192 DC 01-B5 DHU_OPOG_COPY  
0193 . C.                  ¢¢[HK1_TI_CMD_NUM]                EQ    1COUNTUP
```

0194	C.			
0195	+ . TI	2011-10-29 10:50:59.5		
0196	DC	01-B2 DHU_OP_START		
0197	C.	C[HK1_TI_CMD_NUM]	EQ	1COUNTUP
0198	C.			
0199	C.	°Ê²¼□İÄê¾İİÎñİ¥Á¥\$¥Ã¥~¹àİÜ		
0200	C.	C[HK1_TI_CMD_ENA/DIS]	EQ	ENA
0201	C.	C[HK1_TI_CMD_NUM]	EQ	4
0202	C.	C[HK1_NEXT_EXEC_PIM]	EQ	DHU
0203	C.	C[HK1_NEXT_EXEC_DC]	EQ	0xB3
0204	C.			
0205	.	*****		
0206	C.	TIIÎ°è¥À¥Ó¥×		
0207	C.	*****		
0208	C.			
0209	C.	TI_TBL(0x03AB00-0x03AEFF;§ 1024byte)		
0210	+ . DC	01-23 DHU_DMA_DMP_PRM_SET		
0211	BC	(03 ab 03 01 02)		
0212	C.	C[HK1_DMP_TOP_ADRS_1]	EQ	07
0213	C.	C[HK1_DMP_TOP_ADRS_0]	EQ	2B
0214	C.	C[HK1_DMP_BLOCK_NUM]	EQ	3
0215	C.	C[HK1_DMP_REPEAT_NUM]	EQ	0
0216	C.	C[HK1_DMA_DMP_PIM]	EQ	DHU
0217	+ . DC	01-22 DHU_MODE_CHNG		
0218	BC	(07 0b f8)		
0219	C.	C[HK1_PKT_FORM_NO]	EQ	7
0220	C.	C[HK1_PKT_GEN_TIME]	EQ	0.25 s
0221	C.	C[HK1_S_TLM_BIT_RATE]	EQ	32k
0222	C.	C[HK1_X_TLM_BIT_RATE]	EQ	4M
0223	C.	C[HK1_DMP_CHK_FLG]	EQ	EXEC
0224	C.			
0225	. C.	¥À¥Ó¥×½ªİ»ð³İÇ\$		
0226	C.	C[HK1_DMP_CHK_FLG]	EQ	NON
0227	C.			
0228	. C.	RAM ID=TI_TBL◻İ%È¹Ç•è²İOK◻ð³İÇ\$		
0229	C.			
0230	. C.	DHU¥âı¼¥É;Ê¼Ÿ½, ¥łı¼¥Ë;Ė◻òİá◻¹		
0231	+ . DC	01-22 DHU_MODE_CHNG		
0232	BC	(02 0a f8)		
0233	C.	C[HK1_PKT_FORM_NO]	EQ	2
0234	C.	C[HK1_PKT_GEN_TIME]	EQ	0.5S
0235	C.	C[HK1_S_TLM_BIT_RATE]	EQ	32K
0236	C.	C[HK1_X_TLM_BIT_RATE]	EQ	4M
0237	C.			
0238	. C.	Stop EIS observation and temporarily disable EIS mode changes		
0239	C.			
0240	C.			
0241	C.	***** Start EIS operation (TI set) *****		
0242	C.	Execute, after the success of OP upload.		
0243	C.	Set EIS TI-commands		
0244	+ . TI	2011-10-29 10:50:30.0		
0245	DC	07-FC EIS_MODE_MANU		
0246	BC	(21 02)		
0247	+ . TI	2011-10-29 10:50:40.0		
0248	DC	07-FC EIS_MODE_CHG_DIS		
0249	BC	(22)		
0250	. C.	[] [HK1_TI_CMD_NUM] EQ 2 COUNTUP		
0251	C.	***** End EIS operation (TI set) *****		
0252	C.			
0253	C.			
0254	C.	*****		
0255	C.	SOT TI command set		
0256	C.	*****		
0257	C.	Execute, after the success of OP upload.		
0258	+ . TI	2011-10-29 10:50:16.0		
0259	DC	07-F0 MDP_SOT_MODE_STBY		
0260	BC	(41)		
0261	. C.	-----		
0262	C.	HK1_TI_CMD_NUM = 1 CNTUP []		
0263	C.	-----		
0264	C.	***** SOT END *****		
0265	C.			
0266	C.	***** XRT START *****		
0267	C.	Execute, after the success of OP upload.		
0268	+ . TI	2011-10-29 10:50:00.0		
0269	DC	07-F0 MDP_XRT_MODE_STBY		
0270	BC	(c3)		
0271	. C.	[] [HK1_TI_CMD_NUM] EQ 1COUNTUP		
0272	C.			
0273	C.	***** XRT END *****		
0274	C.			
0275	. C.	***** MDP `üÃİîİ»ö¼Ÿ◻ĖÂĐ◻¹◻ēDCBC•×²è *****		
0276	C.	(%ā°İ¥Ö¥Ã¥Ė¥Đ¥Ė¥ā¥Ç¥Ė◻Ė¾¼◻◻Å»ü◻¹◻ē)		
0277	. S.	DC-BC dcbc-402:DCBC		
0278		(MDP_known_event)		
0279	C.			
0280	C.			
0281	. C.	***** ¥Đ¥¹•İ Daily±¿İÎ◻Ė´Ø◻¹◻ēDCBC•×²è *****		
0282	. S.	DC-BC dcbc-153:DCBC		
0283		(SPECIAL-CMD_DAILY_OPERATIN_DCB)		
0284	C.			
0285	C.			
0286	. C.	j āLOS¥Á¥\$¥Ã¥¼Å»Üj ä		
0287	C.			
0288	. C.	***** LOS *****		
0289	C.			

```

main-428 2011-10-29 12:42:08 82 33 SOLAR-B MAIN //
0001 C.
0002 C. ***** AOS *****
0003 C.
0004 C. iãAOS¥Á¥$¥Ã¥¬¼Á»Üjã
0005 C.
0006 C. ¥Ã¥ßj¼¥³¥p¥ó¥ÉÁ÷¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 C. ***** AOCS : Reload orbital element (send every contact) *****
0010 C. ĀījĒ□¿Á□•μ°Æ»Ī×ÁÇ□Ī¥Ç¥Ã¥×¥īj¼¥ĒjĒĒ½μ•īĒjĒ□Ē¼°Ç□□•□¿¼ī¹Ç□īÇÀ®, ū□¹□Ē□□□ÇÁ÷¿®□•□Ē□□□³□Ēj£
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 C. ***** AOCS Commands (Tracking Curve Upload) *****
0015 C. Upload the Orbit Element and the Target Attitude
0016 C. RAM-ID:TARGET_ATT
0017 S. RAM ram-150:TARGET_ATT
0018 C.
0019 C.
0020 C.
0021 C. Set the dump memory area of TARGET_ATT
0022 +. DC 02-48 AOCU_DUMP_SET
0023 BC (07 00 00 00 18 00)
0024 C.
0025 C. <A_STS1>[MEMORY OPERATE SATUS] ADRS = 070000 [ ]
0026 C.
0027 C.
0028 C. Change the TLMFormatNo for the AOCS Dump Format
0029 +. DC 01-22 DHU_MODE_CHNG
0030 BC (04 0b f8)
0031 C.
0032 C. Wait for AOCS DUMP to end
0033 C.
0034 C. Check the dump memory
0035 C.
0036 C. Result = OK [ ]
0037 C.
0038 +. DC 01-22 DHU_MODE_CHNG
0039 BC (02 0a f8)
0040 C.
0041 C. <A_***>[TLM STS] FMT = 2 [ ]
0042 C.
0043 +. DC 02-8E AOCU_ORB_UPD
0044 C.
0045 C. Load OBSTBL, dump OBSTBL, enable EIS mode changes
0046 +. DC 07-FC EIS_MODE_MANU
0047 BC (21 02)
0048 C. Verify EIS in MANUAL mode
0049 C. Estimated OBSTBL upload time is 19s
0050 C. *****
0051 C. EIS START OBSTBL LOAD
0052 C. *****
0053 S. RAM ram-820:EIS_OBSTBL
0054 C.
0055 +. DC 07-FC EIS_DUMP_OBSTBL
0056 BC (07 07 07 00 00 70 00)
0057 C.
0058 C. Execute, after the success of OBSTBL upload.
0059 C. Set EIS TI-commands
0060 +. TI 2011-10-29 10:50:50.0
0061 DC 07-FC EIS_MODE_CHG_ENA
0062 BC (20)
0063 C. [ ] [HK1_TI_CMD_NUM] EQ 1 COUNTUP
0064 C. *****
0065 C. EIS END OBSTBL LOAD
0066 C. *****
0067 C.
0068 C. ***** MDP `ŪĀĪ□Ī»Ō¼Ÿ□ĒĀ□¹□ĒDCBC•×²Ē *****
0069 C. (¼Ā°ĪŸŌ¼Ÿ¥Ē¥p¥Ē¥Ē¥Ç¥ĒĒ½¼□□¼A»Ū□¹□Ē)
0070 S. DC-BC dcbc-402:DCBC
0071 (MDP_known_event)
0072 C.
0073 C.
0074 C. ***** ¥Đ¥¹•Ī Daily±¿ĪŃ□Ē´Ō¹□ĒĒDCBC•×²Ē *****
0075 S. DC-BC dcbc-153:DCBC
0076 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0077 C.
0078 C.
0079 C. iãLOS¥Á¥$¥Ã¥¬¼Á»Üjã
0080 C.
0081 C. ***** LOS *****
0082 C.

```

```
main-429 2011-10-29 12:42:09 208 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. jãAOS¥Á¥$¥Ã¥¬¼Ä»Üjã
0005 C.
0006 C. ¥Ä¥ßj¼¥³¥Ð¥Ó¥ÉÄ÷¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCS : Reload orbital element (send every contact) *****
0010 C. ÄjijË□¿□Ä□•µ°Æ»I×AÇ□I¥¢¥Ä¥×¥ij¼¥ÉjËËè½µ•îÊjËÈ¼°Ç□□•□¿½¹Ç□IjÇÄ®, ù□¹□è□□ÇÄ÷¿®□•□Ê□□³□èj£
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 . C. *****
0015 C. XÄ÷¿®µjON
0016 C. *****
0017 C. ¢´ °ÆÄ, I×ÊÝ□äLOS□□Ç□I»þ´Ö□ð¹íî, □•jÇÉÔI×□EXÄÓON□I¹Ö□Ê□i□Ê□□³□èj£
0018 C.
0019 +. DC 03-B4 TCIA_XPA_ON/HI
0020 M. WAIT_SEC 1
0021 + DC 03-84 TCIA_XMOD_ON
0022 M. WAIT_SEC 1
0023 + DC 03-95 TCIA_XMOD_QPSK
0024 C. ¢¢[HK1_XPA_ON/OFF] EQ ON
0025 C. ¢¢[HK1_XPA_PWR_HI/L0] EQ HI
0026 C. ¢¢[HK1_XMOD_ON/OFF] EQ ON
0027 C. ¢¢[HK1_XMOD_QPSK/PM] EQ QPSK
0028 C.
0029 . C. X¥Ð¥Ó¥É¥i¥Ä¥¬¼ÖÄÖ□¬¼ÄÄê□•□¿□éj¢°Ê²¼□î°ÆÄ, ¼ê½Ç□ð¼Ä¹Ö□¹□èj£
0030 C.
0031 . C. *****
0032 C. DR PT1 Äî¾i°ÆÄ
0033 C. *****
0034 C. ¢´ RESTARTjÊPT1jË□•□¿□□½¹Ç□Ij¢°Ê²¼□î¾Ä¹Ö□»□°j¢DCBC-150□Ø¿Ê□àj£
0035 C.
0036 . C. jãPT1°ÆÄ, ³«»îjã
0037 +. DC 01-29 DHU_S/X_VC4_OFF
0038 + DC 06-C8 DR_PT1_REP_SEL
0039 BC (01 00)
0040 + DC 06-B3 DR_REP_START
0041 + DC 01-32 DHU_X_VC4_ON
0042 C. ¢¢[HK1_REP_PT_1/2] EQ PT1 (¼Ä¹Ö, j¾Ú)
0043 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¾Ú)
0044 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¾Ú)
0045 C.
0046 . C. jã¥¢¥ó¥Æ¥ÊÄÜÄØjÊÄ•Äº²ÖÈðjË, ä□î°ÆÄ, °Æ³«jã
0047 +. DC 06-B3 DR_REP_START
0048 + DC 01-32 DHU_X_VC4_ON
0049 C. ¢¢[HK1_REP_PT_1/2] EQ PT1 (¼Ä¹Ö, j¾Ú)
0050 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¾Ú)
0051 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¾Ú)
0052 C.
0053 C.
0054 . C. PT1°ÆÄ, □¬¼«Æ°Ää»ß□•□¿, äj¢°Ê²¼□ð¼Ä¹Ö□¹□èj£
0055 C. ¥¢¥ó¥Æ¥ÊÄÜÄØ□äÄ•Äº²ÖÈð¬¼á□□½¹Ç□I´°î»□¹□è□□ÇÄÖ□Äj£
0056 C.
0057 . C. *****
0058 C. DR PT2 Äî¾i°ÆÄ
0059 C. *****
0060 C. ¢´ RESTARTjÊPT2jË□•□¿□□½¹Ç□Ij¢°Ê²¼□î¾Ä¹Ö□»□°j¢DCBC-151□Ø¿Ê□àj£
0061 C.
0062 . C. jãPT2°ÆÄ, ³«»îjã
0063 +. DC 01-29 DHU_S/X_VC4_OFF
0064 + DC 06-C8 DR_PT2_REP_SEL
0065 BC (02 00)
0066 + DC 06-B3 DR_REP_START
0067 + DC 01-32 DHU_X_VC4_ON
0068 C. ¢¢[HK1_REP_PT_1/2] EQ PT2 (¼Ä¹Ö, j¾Ú)
0069 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¾Ú)
0070 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¾Ú)
0071 C.
0072 . C. jã¥¢¥ó¥Æ¥ÊÄÜÄØjÊÄ•Äº²ÖÈðjË, ä□î°ÆÄ, °Æ³«jã
0073 +. DC 06-B3 DR_REP_START
0074 + DC 01-32 DHU_X_VC4_ON
0075 C. ¢¢[HK1_REP_PT_1/2] EQ PT2 (¼Ä¹Ö, j¾Ú)
0076 C. ¢¢[HK1_REP_STA/STP] EQ START (¼Ä¹Ö, j¾Ú)
0077 C. ¢¢[HK1_X_VC4_ON/OFF] EQ ON (¼Ä¹Ö, j¾Ú)
0078 C.
0079 . C. *****
0080 C. DR°ÆÄ, Ää»ßj¢XÄ÷¿®µjOFF
0081 C. *****
0082 C.
0083 . C. jãDR°ÆÄ, Ää»ßjã
0084 +. DC 06-B4 DR_REP_STOP
0085 + DC 01-29 DHU_S/X_VC4_OFF
0086 C. ¢¢[HK1_REP_STA/STP] EQ STOP
0087 C. ¢¢[HK1_S_VC4_ON/OFF] EQ OFF
0088 C. ¢¢[HK1_X_VC4_ON/OFF] EQ OFF
0089 C.
0090 . C. jãXÄ÷¿®µjOFFjã
0091 +. DC 03-85 TCIA_XMOD_OFF
0092 M. WAIT_SEC 1
0093 + DC 03-B5 TCIA_XPA_OFF
0094 C. ¢¢[HK1_XMOD_ON/OFF] EQ OFF
0095 C. ¢¢[HK1_XPA_ON/OFF] EQ OFF
```

```

0096 C.
0097 C.
0098 C. *****
0099 C. SOT table upload
0100 C. *****
0101 C. < Stop FG table >
0102 +. DC 07-F0 MDP_FG_CTRL_MANU
0103 BC (51)
0104 C. -----
0105 C. MDP_FG_CTRL_MODE = MANU [ ]
0106 C. -----
0107 C.
0108 C. <Upload FG Observation Table>
0109 S. RAM ram-269:MDP_OBS_F
0110 ( )
0111 C.
0112 C. < Dump RAMID=MDP_OBS_F >
0113 +. DC 07-F0 MDP_DUMP_FGTBL
0114 BC (82 07 00 00 00 38 b8)
0115 C. -----
0116 C. MDP_OBS_F verify = OK/NG [ ]
0117 C. -----
0118 C.
0119 C. *****
0120 C. SOT TI command set
0121 C. *****
0122 C. Execute, after the success of TBL upload.
0123 +. TI 2011-10-29 10:50:18.0
0124 DC 07-F0 MDP_SOT_MODE_OBSV
0125 BC (40)
0126 C. -----
0127 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0128 C. -----
0129 C.
0130 C.
0131 C. ***** XRT START *****
0132 C.
0133 +. DC 07-F0 MDP_XRT_CTRL_MANU
0134 BC (c1)
0135 +. DC 07-F0 MDP_XRT_MODE_STBY
0136 BC (c3)
0137 C. ----- Success Verify ? OK / NG ____
0138 C.
0139 C. XRT Obs. Table Upload
0140 S. RAM ram-291:MDP_OBS_X
0141 ( )
0142 C.
0143 +. DC 07-F0 MDP_DUMP_XRTTBL
0144 BC (84 07 00 00 00 3a d4)
0145 C. ----- Comparison Check ? OK / ERR ____
0146 C.
0147 C.
0148 +. DC 07-F0 MDP_XRT_ROI_SET
0149 BC (cd 01 b1 b1 04 04)
0150 +. DC 07-F0 MDP_XRT_ROI_SET
0151 BC (cd 02 b1 b1 08 08)
0152 +. DC 07-F0 MDP_XRT_ROI_SET
0153 BC (cd 03 b1 b1 08 08)
0154 +. DC 07-F0 MDP_XRT_ROI_SET
0155 BC (cd 04 b1 b1 06 06)
0156 +. DC 07-F0 MDP_XRT_ROI_SET
0157 BC (cd 05 85 83 06 06)
0158 +. DC 07-F0 MDP_XRT_ROI_SET
0159 BC (cd 06 85 83 08 08)
0160 +. DC 07-F0 MDP_XRT_ROI_SET
0161 BC (cd 07 80 80 20 20)
0162 +. DC 07-F0 MDP_XRT_ROI_SET
0163 BC (cd 08 80 80 20 08)
0164 +. DC 07-F0 MDP_XRT_ROI_SET
0165 BC (cd 09 80 80 08 20)
0166 +. DC 07-F0 MDP_XRT_ROI_SET
0167 BC (cd 0f 80 80 06 06)
0168 +. DC 07-F0 MDP_XRT_ROI_SET
0169 BC (cd 10 80 80 08 08)
0170 +. DC 07-F0 MDP_XRT_FLD_ENA
0171 BC (d8)
0172 +. DC 07-F0 MDP_XRT_FLRCTRL_ENA
0173 BC (c8)
0174 +. DC 07-F0 MDP_XRT_AEC_RESET
0175 BC (d0)
0176 +. DC 07-F0 MDP_XRT_ARS_DIS
0177 BC (d5)
0178 +. DC 07-F0 MDP_XRT_FLD_RESET
0179 BC (da)
0180 C. ----- Success Verify ? OK / NG ____
0181 C.
0182 C.
0183 C. All OK? Yes--> Please Proceed. / No --> Stop here.
0184 C.
0185 +. DC 07-F0 MDP_XRT_MODE_OBSV
0186 BC (c2)
0187 +. TI 2011-10-29 10:50:02.0
0188 DC 07-F0 MDP_XRT_MODE_OBSV
0189 BC (c2)
0190 C. ----- Success Verify ? OK / NG ____
0191 C.
0192 C. ***** XRT END *****
0193 C.

```

0194 . C. ***** MDP ´ûÃîï»ô%ýðĖâð¹ðĖDCBC•x²è *****
0195 C. (¾ă°î¥ŒŒ¥Ė¥ð¥Ė¥ă¥ċ¥ĕðĖ½¼ð¼Ā»Ŭ¹ðĕ)
0196 . S. DC-BC dcbc-402:DCBC
0197 (MDP_known_event)
0198 C.
0199 C.
0200 . C. ***** ¥Ð¥¹•İ Daily±ċİÑðĖ´Œ¹ðĖDCBC•x²è *****
0201 . S. DC-BC dcbc-153:DCBC
0202 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0203 C.
0204 C.
0205 . C. ĩăLOS¥Ā¥S¥Ā¥¼Ā»Ŭĭă
0206 C.
0207 . C. ***** LOS *****
0208 C.

Oct 29, 11 12:42

XRT_OGLIST_0236.chk

Page 1/4

*** OP Sequence for XRT ***

2011/10/29	11:01:00.0	AOCS_ORe-point_Start_1_OG [0x097]		
		AOCU_NM	5	02-76 03 00 00 00 00
2011/10/29	18:06:30.0	AOCS_ORe-point_Start_2_OG [0x098]		
		AOCU_NM	5	02-76 00 00 00 00 00
2011/10/29	18:16:30.0	AOCS_ORe-point_Start_1_OG [0x097]		
		AOCU_NM	5	02-76 03 00 00 00 00
2011/10/30	05:37:30.0	AOCS_ORe-point_Start_2_OG [0x098]		
		AOCU_NM	5	02-76 00 00 00 00 00
2011/10/30	05:47:30.0	AOCS_ORe-point_Start_1_OG [0x097]		
		AOCU_NM	5	02-76 03 00 00 00 00
2011/10/30	18:30:00.0	AOCS_ORe-point_Start_2_OG [0x098]		
		AOCU_NM	5	02-76 00 00 00 00 00
2011/10/30	18:40:00.0	AOCS_ORe-point_Start_1_OG [0x097]		
		AOCU_NM	5	02-76 03 00 00 00 00
2011/10/31	05:58:30.0	AOCS_ORe-point_Start_2_OG [0x098]		
		AOCU_NM	5	02-76 00 00 00 00 00
2011/10/31	06:08:30.0	AOCS_ORe-point_Start_1_OG [0x097]		
		AOCU_NM	5	02-76 03 00 00 00 00
2011/10/31	09:25:54.0	XRT_CTRL_MANU_400_OG [0x190]		
		MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/10/31	09:25:56.0	XRT_FOCUS_POSITION_409_OG [0x199]		
		XRT_FOCUS_POSITION	4	07-F8 22 fe 97 00
2011/10/31	09:26:16.0	XRT_FLD_ENA_411_OG [0x19b]		
		MDP_XRT_FLD_ENA	1	07-F0 d8
2011/10/31	09:26:18.0	XRT_FLRCTRL_ENA_413_OG [0x19d]		
		MDP_XRT_FLRCTRL_ENA	1	07-F0 c8
2011/10/31	09:26:20.0	XRT_AEC_RESET_443_OG [0x1bb]		
		MDP_XRT_AEC_RESET	1	07-F0 d0
2011/10/31	09:26:22.0	XRT_ARS_DIS_427_OG [0x1ab]		
		MDP_XRT_ARS_DIS	1	07-F0 d5
2011/10/31	09:28:54.0	XRT_FLD_RESET_412_OG [0x19c]		
		MDP_XRT_FLD_RESET	1	07-F0 da
2011/10/31	09:28:56.0	XRT_QT_PROG_SET_444_OG [0x1bc]		
		MDP_XRT_QT_PROG_SET	2	07-F0 c4 05
2011/10/31	09:28:58.0	XRT_FL_PROG_SET_420_OG [0x1a4]		
		MDP_XRT_FL_PROG_SET	2	07-F0 c5 0d
2011/10/31	09:29:00.0	XRT_CTRL_AUTO_406_OG [0x196]		
		MDP_XRT_CTRL_AUTO	1	07-F0 c0
2011/10/31	10:03:30.0	XRT_CTRL_MANU_408_OG [0x198]		
		MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/10/31	10:03:32.0	XRT_FLD_RESET_412_OG [0x19c]		
		MDP_XRT_FLD_RESET	1	07-F0 da
2011/10/31	10:03:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]		
		MDP_XRT_PREFLR_STRT	1	07-F0 e8
2011/10/31	10:06:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]		
		MDP_XRT_PREFLR_STOP	1	07-F0 e9
2011/10/31	10:16:30.0	XRT_Custom_418_OG [0x1a2]		
2011/10/31	10:17:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]		
		MDP_XRT_CTRL_AUTO	1	07-F0 c0
2011/10/31	13:56:54.0	XRT_CTRL_MANU_400_OG [0x190]		
		MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/10/31	13:56:56.0	XRT_FOCUS_POSITION_409_OG [0x199]		
		XRT_FOCUS_POSITION	4	07-F8 22 fe 97 00
2011/10/31	13:57:16.0	XRT_FLD_ENA_411_OG [0x19b]		
		MDP_XRT_FLD_ENA	1	07-F0 d8
2011/10/31	13:57:18.0	XRT_FLRCTRL_ENA_413_OG [0x19d]		
		MDP_XRT_FLRCTRL_ENA	1	07-F0 c8
2011/10/31	13:57:20.0	XRT_AEC_RESET_443_OG [0x1bb]		
		MDP_XRT_AEC_RESET	1	07-F0 d0
2011/10/31	13:57:22.0	XRT_ARS_DIS_427_OG [0x1ab]		
		MDP_XRT_ARS_DIS	1	07-F0 d5
2011/10/31	13:59:54.0	XRT_FLD_RESET_412_OG [0x19c]		
		MDP_XRT_FLD_RESET	1	07-F0 da
2011/10/31	13:59:56.0	XRT_QT_PROG_SET_407_OG [0x197]		
		MDP_XRT_QT_PROG_SET	2	07-F0 c4 02
2011/10/31	13:59:58.0	XRT_FL_PROG_SET_420_OG [0x1a4]		
		MDP_XRT_FL_PROG_SET	2	07-F0 c5 0d
2011/10/31	14:00:00.0	XRT_CTRL_AUTO_406_OG [0x196]		
		MDP_XRT_CTRL_AUTO	1	07-F0 c0
2011/10/31	15:26:30.0	XRT_CTRL_MANU_408_OG [0x198]		
		MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/10/31	15:26:32.0	XRT_FLD_RESET_412_OG [0x19c]		
		MDP_XRT_FLD_RESET	1	07-F0 da
2011/10/31	15:26:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]		
		MDP_XRT_PREFLR_STRT	1	07-F0 e8
2011/10/31	15:29:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]		
		MDP_XRT_PREFLR_STOP	1	07-F0 e9
2011/10/31	15:50:00.0	XRT_Custom_418_OG [0x1a2]		
2011/10/31	15:51:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]		
		MDP_XRT_CTRL_AUTO	1	07-F0 c0
2011/10/31	17:03:00.0	XRT_CTRL_MANU_408_OG [0x198]		
		MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/10/31	17:03:02.0	XRT_FLD_RESET_412_OG [0x19c]		
		MDP_XRT_FLD_RESET	1	07-F0 da
2011/10/31	17:03:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]		
		MDP_XRT_PREFLR_STRT	1	07-F0 e8
2011/10/31	17:06:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]		
		MDP_XRT_PREFLR_STOP	1	07-F0 e9
2011/10/31	17:26:30.0	XRT_Custom_418_OG [0x1a2]		
2011/10/31	17:27:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]		
		MDP_XRT_CTRL_AUTO	1	07-F0 c0

Saturday October 29, 2011

1/4

Oct 29, 11 12:42

XRT_OGLIST_0236.chk

Page 2/4

2011/10/31	17:59:54.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	17:59:56.0	XRT_FOCUS_POSITION_401_OG [0x191]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00
2011/10/31	18:00:00.0	AOCS_ORe-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	00 00 00 00 00
2011/10/31	18:00:16.0	XRT_FLD_DIS_402_OG [0x192]	MDP_XRT_FLD_DIS	1	07-F0	d9
2011/10/31	18:00:18.0	XRT_FLRCTRL_DIS_433_OG [0x1b1]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9
2011/10/31	18:00:20.0	XRT_ARS_DIS_438_OG [0x1b6]	MDP_XRT_ARS_DIS	1	07-F0	d5
2011/10/31	18:02:58.0	XRT_QT_PROG_SET_436_OG [0x1b4]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 04
2011/10/31	18:03:00.0	XRT_CTRL_AUTO_406_OG [0x196]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/10/31	18:09:54.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	18:09:56.0	XRT_FOCUS_POSITION_409_OG [0x199]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2011/10/31	18:10:00.0	AOCS_ORe-point_Start_3_OG [0x099]	AOCU_NM	5	02-76	00 10 e5 53 74
2011/10/31	18:10:16.0	XRT_FLD_ENA_411_OG [0x19b]	MDP_XRT_FLD_ENA	1	07-F0	d8
2011/10/31	18:10:18.0	XRT_FLRCTRL_ENA_413_OG [0x19d]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2011/10/31	18:10:20.0	XRT_AEC_RESET_443_OG [0x1bb]	MDP_XRT_AEC_RESET	1	07-F0	d0
2011/10/31	18:10:22.0	XRT_ARS_DIS_427_OG [0x1ab]	MDP_XRT_ARS_DIS	1	07-F0	d5
2011/10/31	18:12:54.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	18:12:56.0	XRT_QT_PROG_SET_444_OG [0x1bc]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 05
2011/10/31	18:12:58.0	XRT_FL_PROG_SET_420_OG [0x1a4]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 0d
2011/10/31	18:13:00.0	XRT_CTRL_AUTO_406_OG [0x196]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/10/31	18:40:00.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	18:40:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	18:40:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/10/31	18:43:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/10/31	19:03:30.0	XRT_Custom_418_OG [0x1a2]				
2011/10/31	19:04:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/10/31	20:17:00.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	20:17:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	20:17:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/10/31	20:20:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/10/31	20:40:30.0	XRT_Custom_418_OG [0x1a2]				
2011/10/31	20:41:30.0	XRT_CTRL_AUTO_419_OG [0x1a3]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/10/31	21:54:30.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	21:54:32.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	21:54:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/10/31	21:57:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/10/31	22:17:00.0	XRT_Custom_418_OG [0x1a2]				
2011/10/31	22:18:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/10/31	23:09:54.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	23:09:56.0	XRT_FOCUS_POSITION_409_OG [0x199]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2011/10/31	23:10:00.0	AOCS_ORe-point_Start_1_OG [0x097]	AOCU_NM	5	02-76	03 00 00 00 00
2011/10/31	23:10:16.0	XRT_FLD_ENA_411_OG [0x19b]	MDP_XRT_FLD_ENA	1	07-F0	d8
2011/10/31	23:10:18.0	XRT_FLRCTRL_ENA_413_OG [0x19d]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2011/10/31	23:10:20.0	XRT_AEC_RESET_443_OG [0x1bb]	MDP_XRT_AEC_RESET	1	07-F0	d0
2011/10/31	23:10:22.0	XRT_ARS_DIS_427_OG [0x1ab]	MDP_XRT_ARS_DIS	1	07-F0	d5
2011/10/31	23:12:54.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	23:12:56.0	XRT_QT_PROG_SET_444_OG [0x1bc]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 05
2011/10/31	23:12:58.0	XRT_FL_PROG_SET_420_OG [0x1a4]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 0d
2011/10/31	23:13:00.0	XRT_CTRL_AUTO_406_OG [0x196]	MDP_XRT_CTRL_AUTO	1	07-F0	c0

Oct 29, 11 12:42

XRT_OGLIST_0236.chk

Page 3/4

2011/10/31	23:32:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/10/31	23:32:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/10/31	23:32:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/10/31	23:35:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/10/31	23:44:00.0	XRT_Custom_418_OG [0x1a2]			
2011/10/31	23:45:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	01:00:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	01:00:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/11/01	01:00:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/11/01	01:03:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/11/01	01:15:00.0	XRT_Custom_418_OG [0x1a2]			
2011/11/01	01:16:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	02:31:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	02:31:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/11/01	02:31:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/11/01	02:34:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/11/01	02:51:30.5	XRT_Custom_418_OG [0x1a2]			
2011/11/01	02:52:30.5	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	03:59:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	03:59:32.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/11/01	03:59:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/11/01	04:02:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/11/01	04:29:00.0	XRT_Custom_418_OG [0x1a2]			
2011/11/01	04:30:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	05:40:00.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	05:40:02.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/11/01	05:40:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2011/11/01	05:43:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2011/11/01	06:16:24.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	06:16:26.0	XRT_FOCUS_POSITION_401_OG [0x191]			
		XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00
2011/11/01	06:16:30.0	AOCS_Ore-point_Start_2_OG [0x098]			
		AOCU_NM	5	02-76	00 00 00 00 00
2011/11/01	06:16:46.0	XRT_FLD_DIS_402_OG [0x192]			
		MDP_XRT_FLD_DIS	1	07-F0	d9
2011/11/01	06:16:48.0	XRT_FLRCTRL_DIS_433_OG [0x1b1]			
		MDP_XRT_FLRCTRL_DIS	1	07-F0	c9
2011/11/01	06:16:50.0	XRT_ARS_DIS_438_OG [0x1b6]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2011/11/01	06:19:28.0	XRT_QT_PROG_SET_436_OG [0x1b4]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 04
2011/11/01	06:19:30.0	XRT_CTRL_AUTO_406_OG [0x196]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	06:26:24.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	06:26:26.0	XRT_FOCUS_POSITION_409_OG [0x199]			
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2011/11/01	06:26:30.0	AOCS_Ore-point_Start_1_OG [0x097]			
		AOCU_NM	5	02-76	03 00 00 00 00
2011/11/01	06:26:46.0	XRT_FLD_ENA_411_OG [0x19b]			
		MDP_XRT_FLD_ENA	1	07-F0	d8
2011/11/01	06:26:48.0	XRT_FLRCTRL_ENA_413_OG [0x19d]			
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2011/11/01	06:26:50.0	XRT_AEC_RESET_443_OG [0x1bb]			
		MDP_XRT_AEC_RESET	1	07-F0	d0
2011/11/01	06:26:52.0	XRT_ARS_DIS_427_OG [0x1ab]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2011/11/01	06:29:24.0	XRT_FLD_RESET_412_OG [0x19c]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2011/11/01	06:29:26.0	XRT_QT_PROG_SET_444_OG [0x1bc]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 05
2011/11/01	06:29:28.0	XRT_FL_PROG_SET_420_OG [0x1a4]			
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 0d
2011/11/01	06:29:30.0	XRT_CTRL_AUTO_406_OG [0x196]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2011/11/01	07:20:30.0	XRT_CTRL_MANU_408_OG [0x198]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2011/11/01	07:20:32.0	XRT_FLD_RESET_412_OG [0x19c]			

Saturday October 29, 2011

3/4

Oct 29, 11 12:42

XRT_OGLIST_0236.chk

Page 4/4

2011/11/01	07:20:34.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_FLD_RESET	1	07-F0 da
2011/11/01	07:23:44.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STRT	1	07-F0 e8
2011/11/01	07:44:00.0	XRT_Custom_418_OG [0x1a2]	MDP_XRT_PREFLR_STOP	1	07-F0 e9
2011/11/01	07:45:00.0	XRT_CTRL_AUTO_419_OG [0x1a3]	MDP_XRT_CTRL_AUTO	1	07-F0 c0
2011/11/01	08:45:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/11/01	09:00:00.0	XRT_CTRL_MANU_408_OG [0x198]	MDP_XRT_CTRL_MANU	1	07-F0 c1
2011/11/01	09:00:02.0	XRT_FLD_RESET_412_OG [0x19c]	MDP_XRT_FLD_RESET	1	07-F0 da
2011/11/01	09:00:04.0	XRT_PREFLR_STRT_422_OG [0x1a6]	MDP_XRT_PREFLR_STRT	1	07-F0 e8
2011/11/01	09:03:14.0	XRT_PREFLR_STOP_424_OG [0x1a8]	MDP_XRT_PREFLR_STOP	1	07-F0 e9
2011/11/01	09:53:00.0	AOCS_ORe-point_Start_2_OG [0x098]	AOCU_NM	5	02-76 00 00 00 00 00