

# XRT Timeline to be uploaded on 2013/01/03

Period: 2013/01/03 09:14:00 - 2013/01/08 11:31:00

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## Normal mode

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### XOB #195D: AR Standard-B(Morphology) with PFB 304 FOV, thin-Be + multifilter context, 512x512 at 1064 1048, 24s-cad w/ G-Band VLS Closed Test

Term	Pointing (x, y)	Comment
01/04 09:23:36 - 01/04 14:40:00	Track ( -98.3, -208.4) <sup>01/03 09:24:00</sup>	# OP start + 10min, Emerging AR obs.
<b>PROG= 19 Inf.-time(s)</b>		
└─ Subr= 1 1-time(s) 2.0sec		
└─ Seqn= 98 1-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 16.0s Obs 1x1 512x512 (1064, 1048) Q=98 0 0 2.0sec
└─ Open/G-band	Open/G-band open	Safe Norm 44ms Obs 1x1 512x512 (1064, 1048) Q=98 0 0 2.0sec
└─ Seqn= 31 1-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 1 0 2.0sec
└─ Seqn= 27 4-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Norm 500ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Open/thick-Al	Open/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Al-poly/Open	Al-poly/thick-Be close	Safe Norm 250ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ C-poly/Open	C-poly/thick-Al close	Safe Norm 250ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.00s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ med-Be/Open	med-Be/Open close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ med-Al/Open	med-Al/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Subr= 2 1-time(s) 2.0sec		
└─ Seqn= 25 150-time(s) 2.0sec		
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 6.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 6.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 6.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 3 6.0sec
Default Filter	Thicker Filter VLS	mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

### XOB #195E: AR Standard-B(Morphology) with PFB 304 FOV, thin-Be + multifilter context, 512x512 at 1064 1048, 60s-cad w/ G-Band VLS Closed Test

Term	Pointing (x, y)	Comment
01/04 14:43:06 - 01/04 17:59:54	Track ( -98.3, -208.4) <sup>01/03 09:24:00</sup>	# OP start + 10min, Emerging AR obs.
01/04 18:13:00 - 01/05 06:13:54	Track ( 196.4, -206.7) <sup>01/04 18:10:00</sup>	Cont.
01/05 06:27:00 - 01/05 10:30:00	Track ( 303.0, -207.5) <sup>01/05 06:24:00</sup>	Cont.
<b>PROG= 10 Inf.-time(s)</b>		
└─ Subr= 1 1-time(s) 2.0sec		
└─ Seqn= 98 1-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 16.0s Obs 1x1 512x512 (1064, 1048) Q=98 0 0 2.0sec
└─ Open/G-band	Open/G-band open	Safe Norm 44ms Obs 1x1 512x512 (1064, 1048) Q=98 0 0 2.0sec
└─ Seqn= 31 1-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 1 0 2.0sec
└─ Seqn= 27 4-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Norm 500ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Open/thick-Al	Open/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Al-poly/Open	Al-poly/thick-Be close	Safe Norm 250ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ C-poly/Open	C-poly/thick-Al close	Safe Norm 250ms Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.00s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ med-Be/Open	med-Be/Open close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ med-Al/Open	med-Al/thick-Al close	Safe Norm 16.0s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
└─ Subr= 2 1-time(s) 2.0sec		
└─ Seqn= 99 70-time(s) 2.0sec		
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 15.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 15.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 15.0sec
└─ thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 3 15.0sec
Default Filter	Thicker Filter VLS	mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

### XOB #192F: Synoptic Q95 2x2 - Al/mesh(33/1024) + Dark cal(2x2 4x4 8x8 512 Q98) + Dark cal(1x1 512x2048 -1x1 2048x512) + Ti-poly(64/1443) + Thin-Be(18

Term	Pointing (x, y)	Comment
01/04 18:04:24 - 01/04 18:09:54	Fixed ( 0.0, 0.0)	synoptic
01/05 06:17:00 - 01/05 06:23:54	Fixed ( 0.0, 0.0)	synoptic, shifted 14.0 min
<b>PROG= 13 1-time(s)</b>		
└─ Subr= 1 1-time(s) 14.0sec		
└─ Seqn= 64 1-time(s) 4.0sec		
└─ Open/Al-mesh	Open/Ti-poly close	Safe Norm 32ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
└─ Open/Al-mesh	Open/Ti-poly close	Safe Norm 1.00s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
└─ Seqn= 6 1-time(s) 2.0sec		
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 500ms Obs 2x2 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 500ms Obs 4x4 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 500ms Obs 8x8 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 500ms Obs 1x1 2048x512 (1024, 1024) DPCM 0 0 2.0sec
└─ Open/Ti-poly	Open/thick-Al close	Safe Dark 500ms Obs 1x1 512x2048 (1024, 1024) DPCM 0 0 2.0sec
└─ Seqn= 70 1-time(s) 4.0sec		
└─ Open/Ti-poly	Open/Ti-poly close	Safe Norm 63ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
└─ Open/Ti-poly	Open/Ti-poly close	Safe Norm 1.41s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec

Seqn= 67	1-time(s)	2.0sec																		
thin-Be/Open	thin-Be/Open	close	Safe	Norm	177ms	Obs	2x2	2048x2048	(1024, 1024)	Q=95	0	0	2.0sec							
thin-Be/Open	thin-Be/Open	close	Safe	Norm	2.83s	Obs	2x2	2048x2048	(1024, 1024)	Q=95	0	0	2.0sec							
Seqn= 69	1-time(s)	2.0sec																		
Open/G-band	Open/G-band	open	Safe	Norm	8ms	Obs	2x2	2048x2048	(1024, 1024)	Q=95	0	0	2.0sec							
Subr= 2	1-time(s)	2.0sec																		
Seqn= 68	1-time(s)	2.0sec																		
Open/G-band	Open/G-band	close	Safe	Norm	32ms	Obs	1x1	2048x2048	(1024, 1024)	DPCM	0	0	2.0sec							
Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)			Comp.	AEC Buffer	Interval							

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**Flare mode**

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**XOB #1920: Flare obs. dynamics - thin-Be high cadence + context (med-Al,thick-Be -384x384 + Al-poly 512x512 2x2)-Gband (45ms)-15 loops**

Term	Pointing (x, y)	Comment
01/04 09:23:36 - 01/04 14:40:00	Track ( -98.3, -208.4) <sup>Ⓢ 01/03 09:24:00</sup>	# OP start + 10min, Emerging AR obs.
01/04 14:43:06 - 01/04 17:59:54	Track ( -98.3, -208.4) <sup>Ⓢ 01/03 09:24:00</sup>	# OP start + 10min, Emerging AR obs.
01/04 18:13:00 - 01/05 06:13:54	Track ( 196.4, -206.7) <sup>Ⓢ 01/04 18:10:00</sup>	Cont.
01/05 06:27:00 - 01/05 10:30:00	Track ( 303.0, -207.5) <sup>Ⓢ 01/05 06:24:00</sup>	Cont.

**PROG= 16 15-time(s)**

Subr= 1	45-time(s)	10.0sec																		
Seqn= 35	1-time(s)	2.0sec																		
thin-Be/Open	med-Be/Open	close	Safe	Norm	250ms	Obs	1x1	384x384	(1024, 1024)	Q=95	3	0	2.0sec							
Subr= 2	1-time(s)	10.0sec																		
Seqn= 36	1-time(s)	2.0sec																		
med-Al/Open	med-Al/thick-Al	close	Safe	Norm	500ms	Obs	1x1	384x384	(1024, 1024)	Q=95	3	0	2.0sec							
Open/thick-Be	Open/thick-Be	close	Safe	Norm	2.00s	Obs	1x1	384x384	(1024, 1024)	Q=95	3	0	2.0sec							
Seqn= 37	1-time(s)	2.0sec																		
Al-poly/Open	Al-poly/thick-Al	close	Safe	Norm	125ms	Obs	2x2	512x512	(1024, 1024)	Q=95	2	0	2.0sec							
Seqn= 38	1-time(s)	2.0sec																		
Open/G-band	Open/G-band	open	Safe	Norm	44ms	Obs	1x1	384x384	(1024, 1024)	Q=98	0	0	2.0sec							
Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	1x1	384x384	(1024, 1024)	Q=98	0	0	2.0sec							
Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	2x2	512x512	(1024, 1024)	Q=98	0	0	2.0sec							
Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)			Comp.	AEC Buffer	Interval							

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**Active Region Search**

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NOT USED

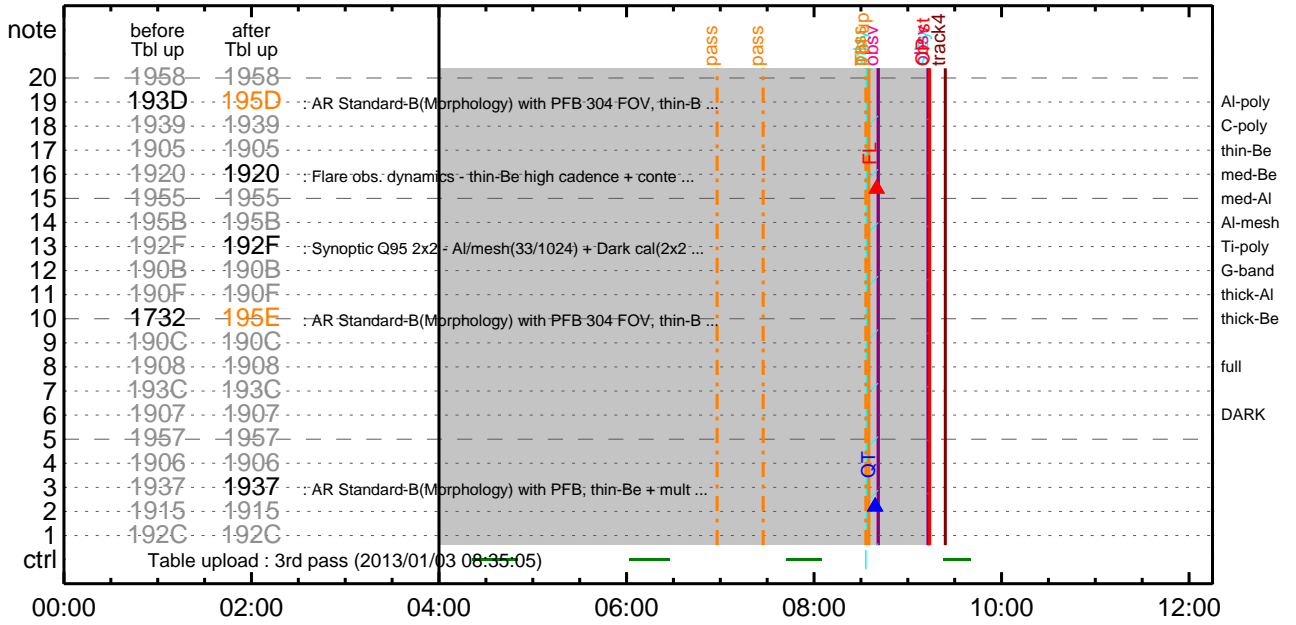
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**Flare Detection**

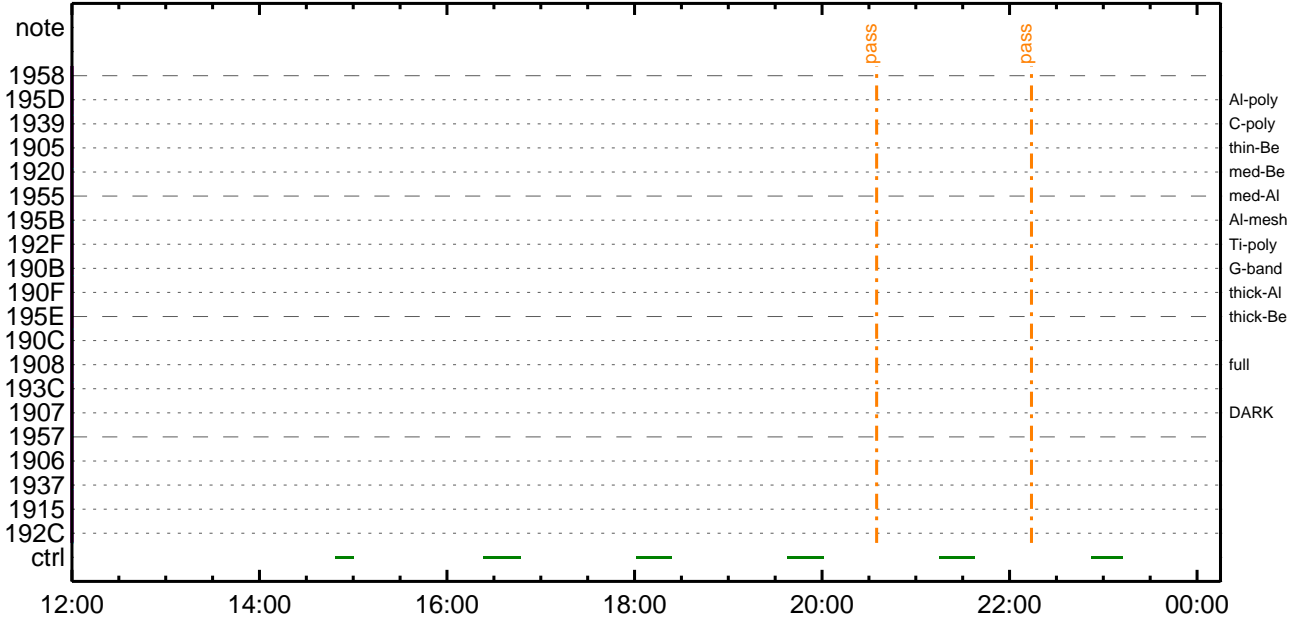
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FLD Patrol													
Term	Pointing (x, y)	Comment											
01/04 18:10:16 - 01/05 06:14:16	Track ( 196.4, -206.7) <sup>Ⓢ 01/04 18:10:00</sup>	Cont.											
01/05 06:24:16 - 01/08 11:31:00	Track ( 303.0, -207.5) <sup>Ⓢ 01/05 06:24:00</sup>	Cont.											
Open/Ti-poly	Open/thick-Al	close	Safe	Norm	8ms	Obs	8x8			Q=50			30sec
Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)			Comp.	AEC Buffer	Interval

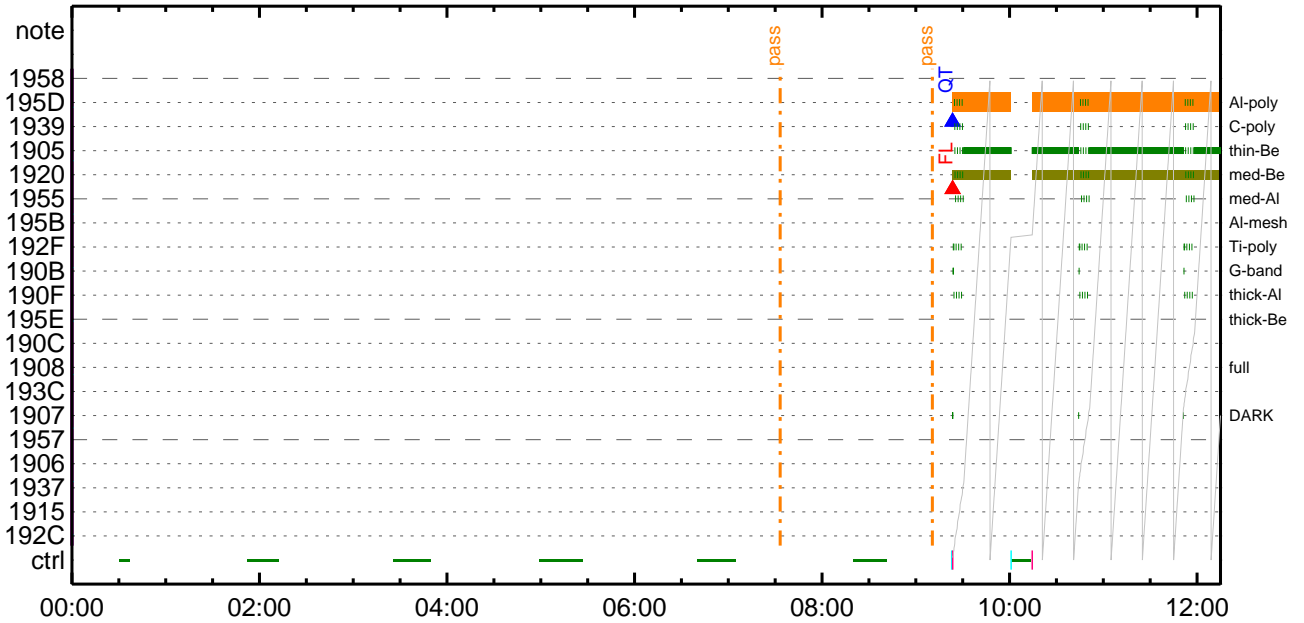
### CMDI #0156 2013/01/03



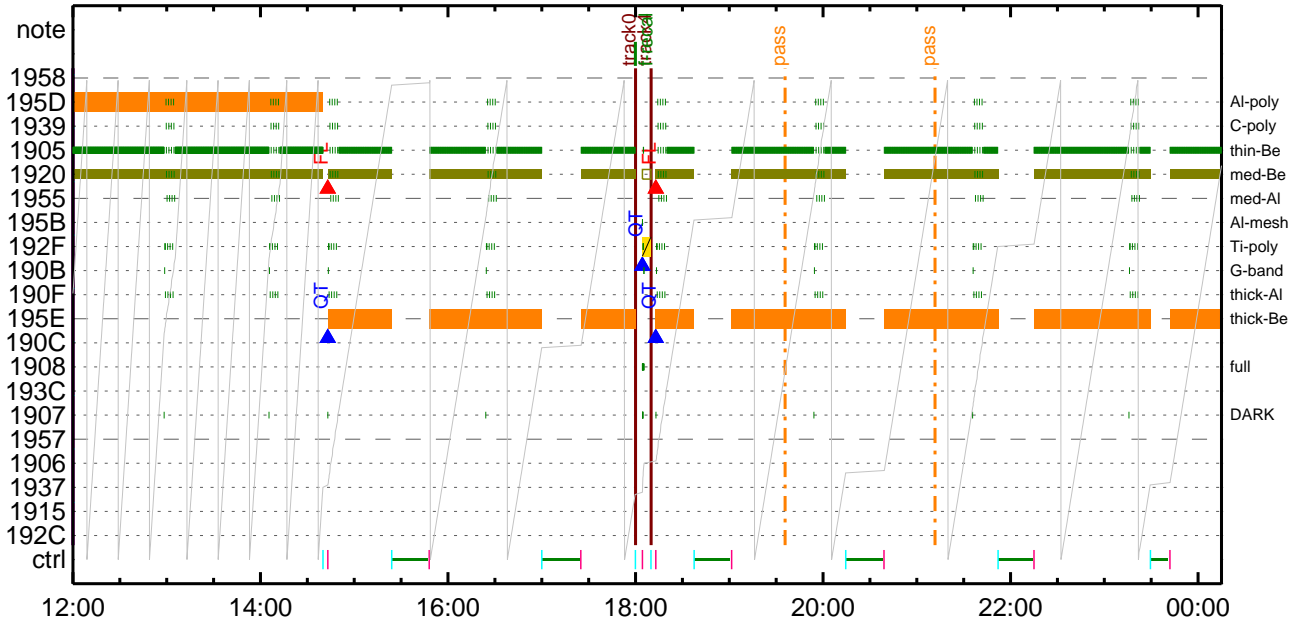
### CMDI #0156 2013/01/03



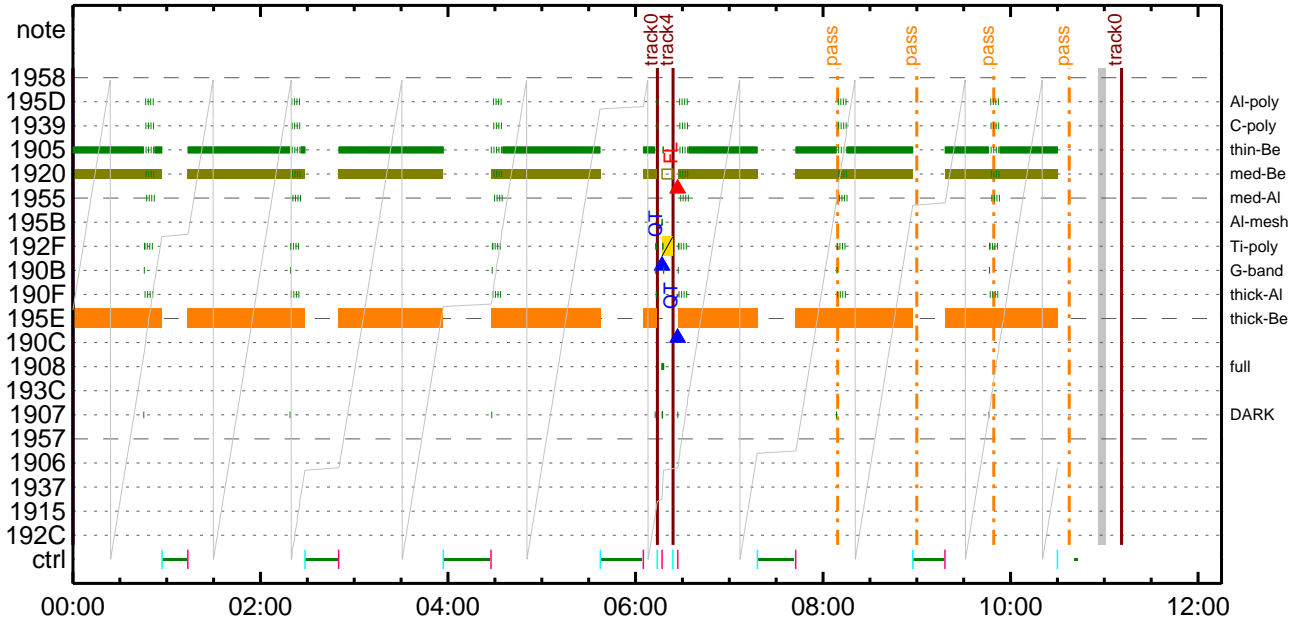
### CMDI #0156 2013/01/04



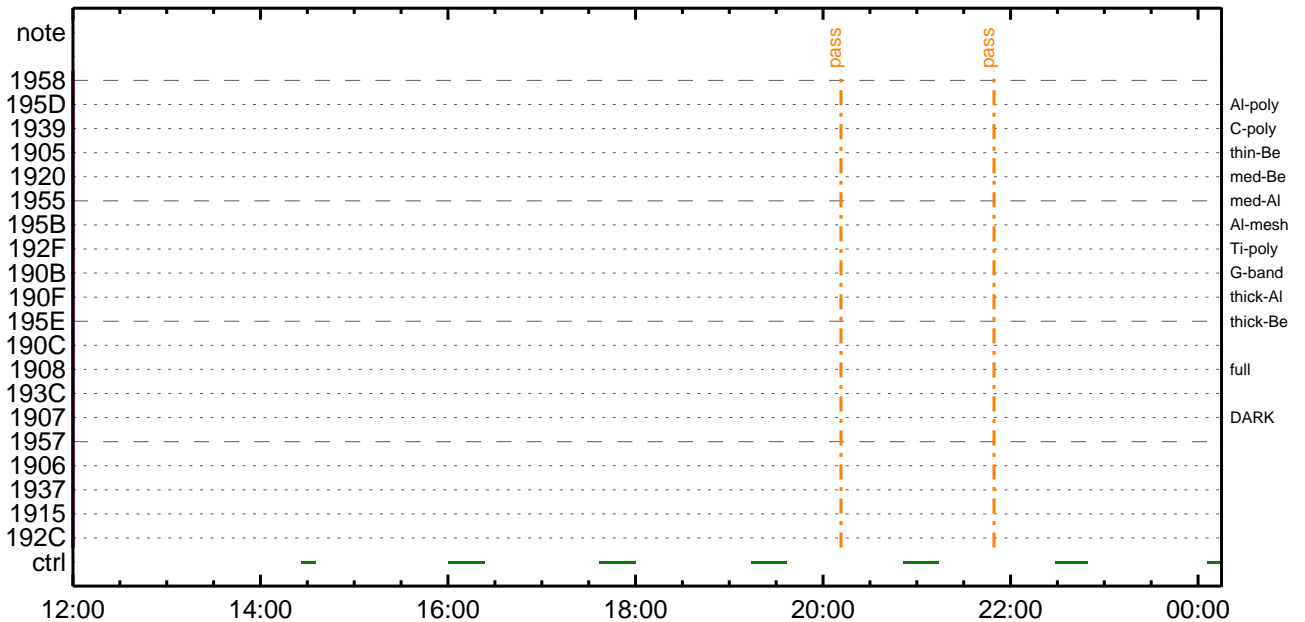
### CMDI #0156 2013/01/04



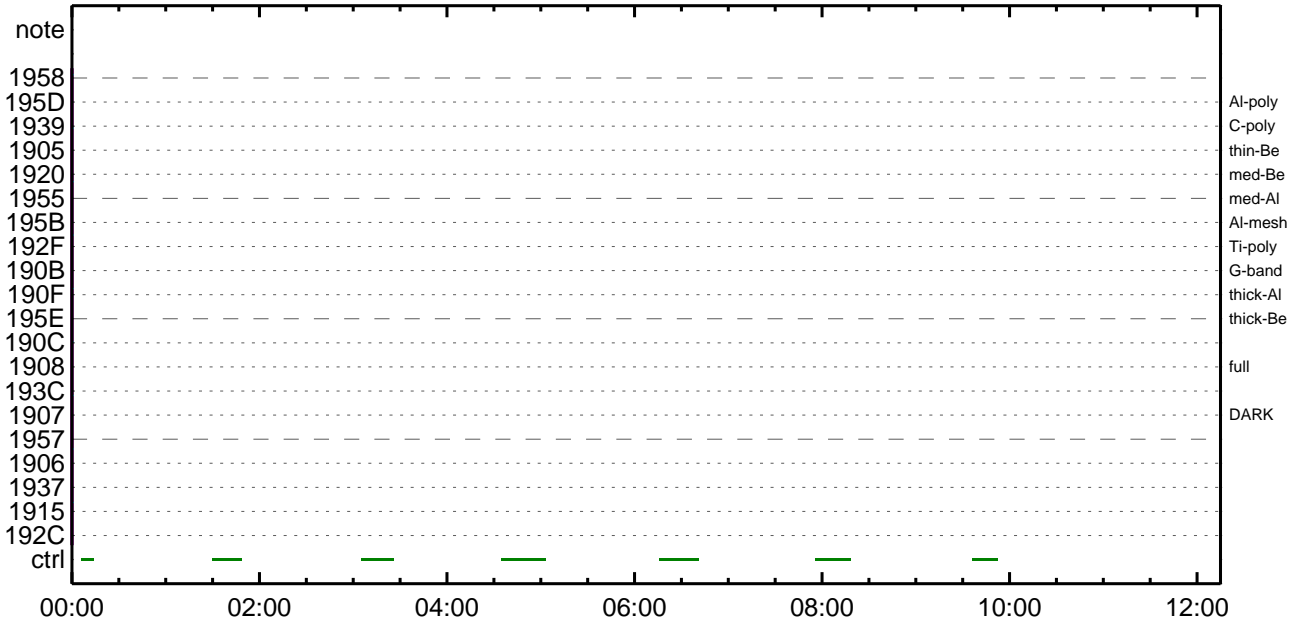
### CMDI #0156 2013/01/05



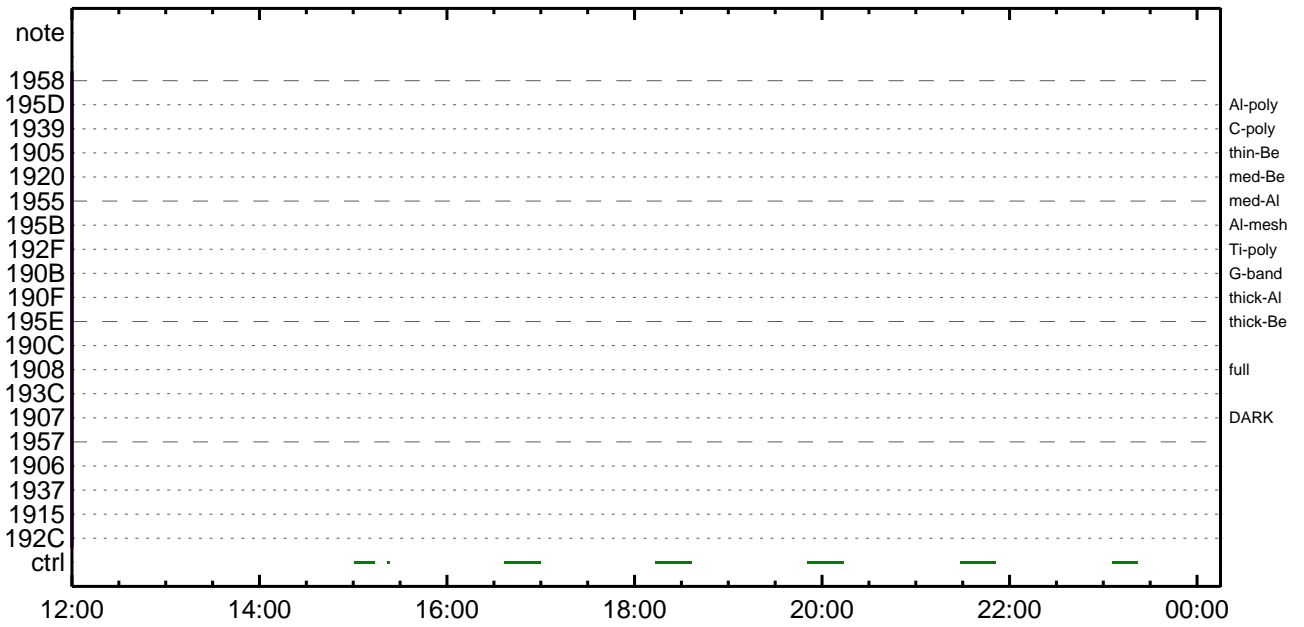
### CMDI #0156 2013/01/05



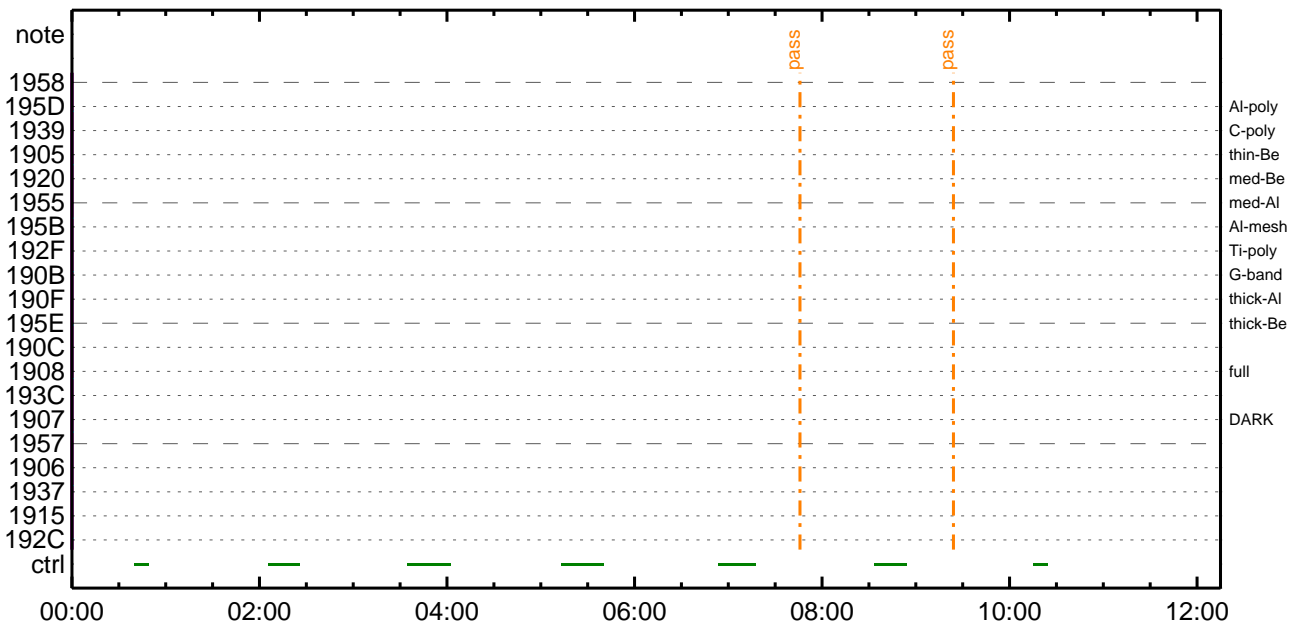
CMDI #0156 2013/01/06



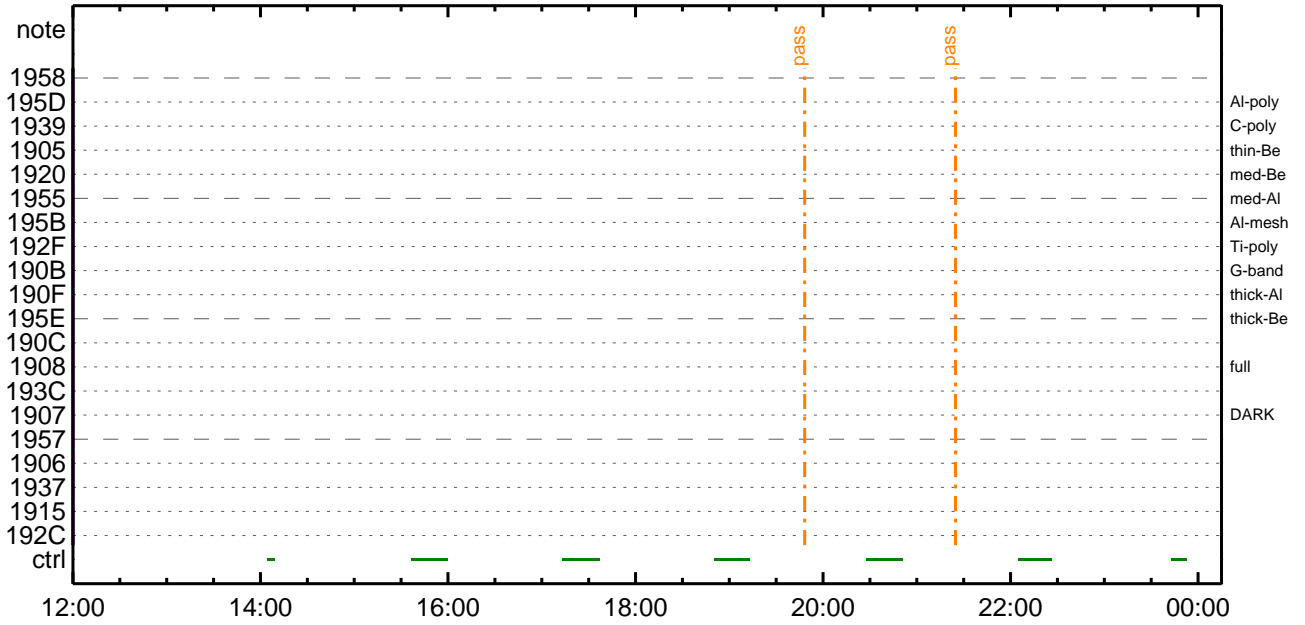
CMDI #0156 2013/01/06



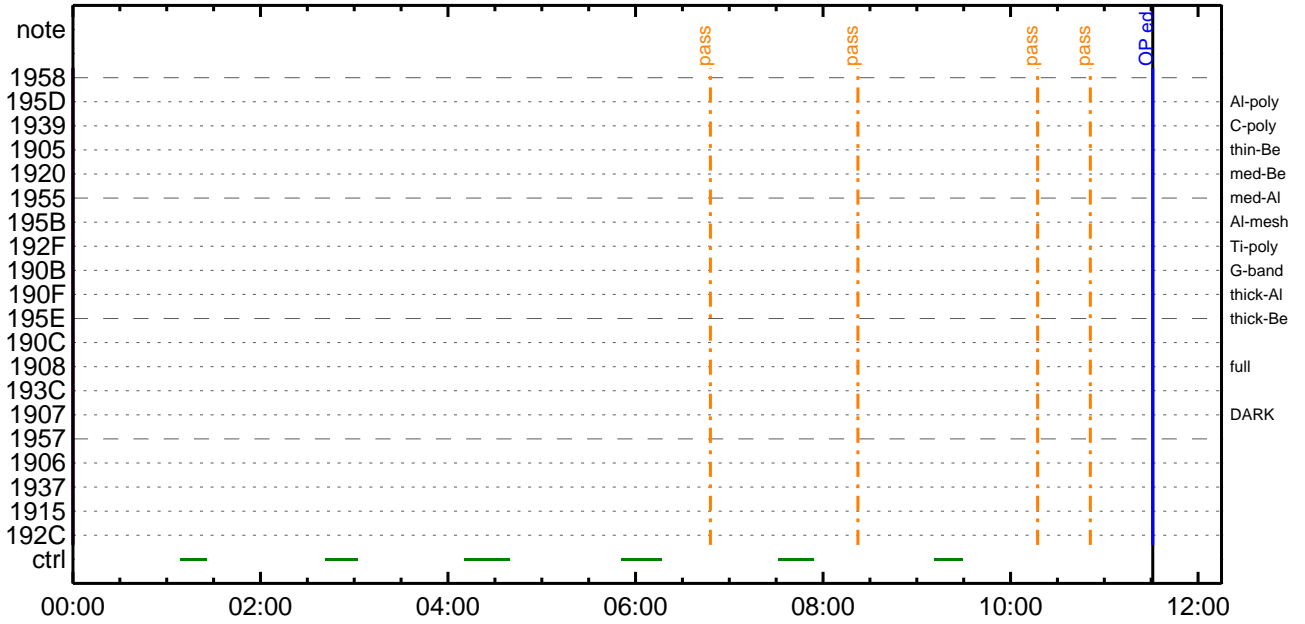
CMDI #0156 2013/01/07



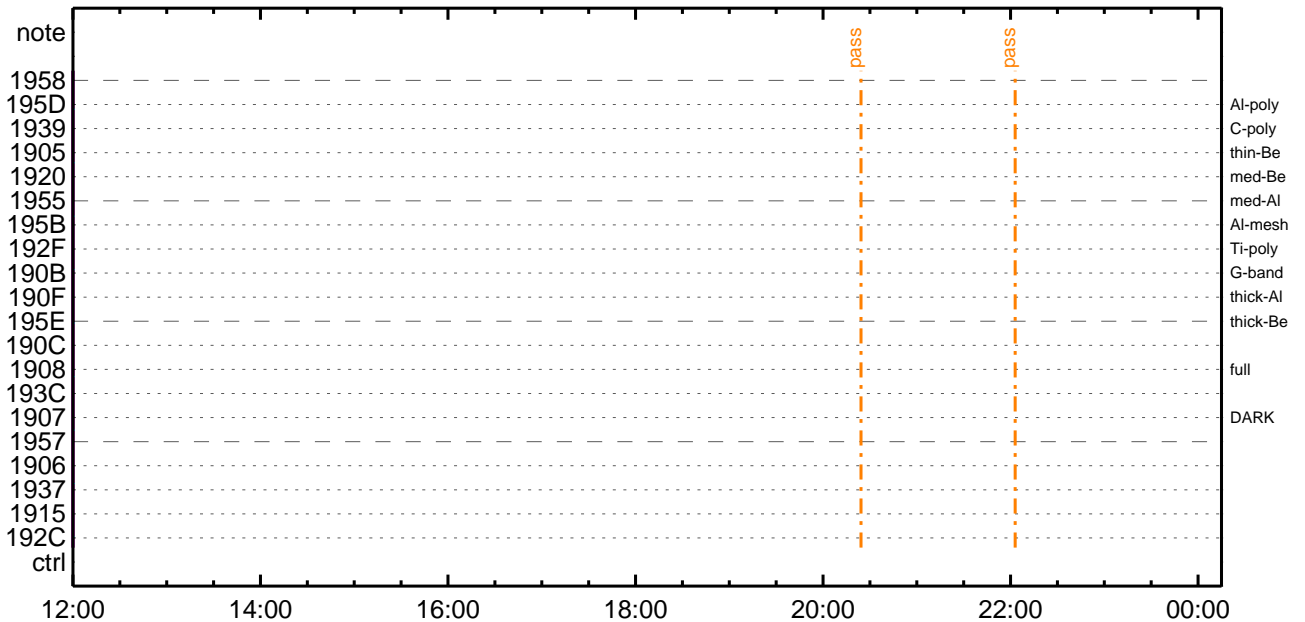
### CMDI #0156 2013/01/07



### CMDI #0156 2013/01/08



### CMDI #0156 2013/01/08





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0096 C.
0097 C.
0098 C. *****
0099 C. OP/OGY1;4YE;|YAYOYx
0100 C. *****
0101 C.
0102 C. ;ãOP/OGY1;4YE;ã
0103 S. OP op-366:OP
0104 ( )
0105 S. OG og-366:OG
0106 ( )
0107 C.
0108 C. ;ãNMOG&OPîî°èYAYOYx;ã
0109 C. NMOG(0x200000-0x207FFF;§ 32 kbyte)
0110 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0111 BC (20 00 7f 01 02)
0112 C. çç[HK1_DMP_TOP_ADRS_1] EQ 40
0113 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0114 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0115 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0116 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0117 +. DC 01-22 DHU_MODE_CHNG
0118 BC (07 0b f8)
0119 C. çç[HK1_PKT_FORM_NO] EQ 7
0120 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0121 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0122 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0123 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0124 C. YAYOYx½ªî»ò³îÇ§
0125 C. çç[HK1_DMP_CHK_FLG] EQ NON
0126 C. RAM ID=NMOG²î¼E¹ç•è²îOKò³îÇ§
0127 C.
0128 C. NMOG(0x208000-0x20FFFF;§ 32 kbyte)
0129 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0130 BC (20 80 7f 01 02)
0131 C. çç[HK1_DMP_TOP_ADRS_1] EQ 41
0132 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0133 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0134 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0135 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0136 +. DC 01-22 DHU_MODE_CHNG
0137 BC (07 0b f8)
0138 C. çç[HK1_PKT_FORM_NO] EQ 7
0139 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0140 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0141 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0142 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0143 C. YAYOYx½ªî»ò³îÇ§
0144 C. çç[HK1_DMP_CHK_FLG] EQ NON
0145 C. RAM ID=NMOG²î¼E¹ç•è²îOKò³îÇ§
0146 C.
0147 C. NMOG(0x210000-0x2100FF;§ 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)
0148 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0149 BC (21 00 41 01 02)
0150 C. çç[HK1_DMP_TOP_ADRS_1] EQ 42
0151 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0152 C. çç[HK1_DMP_BLOCK_NUM] EQ 65
0153 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0154 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0155 +. DC 01-22 DHU_MODE_CHNG
0156 BC (07 0b f8)
0157 C. çç[HK1_PKT_FORM_NO] EQ 7
0158 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0159 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0160 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0161 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0162 C. YAYOYx½ªî»ò³îÇ§
0163 C. çç[HK1_DMP_CHK_FLG] EQ NON
0164 C. RAM ID=NMOG, RAM ID=OP²î¼E¹ç•è²îOKò³îÇ§
0165 C.
0166 C. ***** °E²¼òî¼Ã´¶Á°òEÉ¬ò°Á÷¿@ (¼âµ-YAYOYx½ê¼çòðÁÓÆòÇ¼ª°¬òE¼î¹çòçòâ) *****
0167 C. DHUYâ;4YE;E¼Y½, Yî;4YE;Eòðîã¹
0168 +. DC 01-22 DHU_MODE_CHNG
0169 BC (02 0a f8)
0170 C. çç[HK1_PKT_FORM_NO] EQ 2
0171 C. çç[HK1_PKT_GEN_TIME] EQ 0.5S
0172 C. çç[HK1_S_TLM_BIT_RATE] EQ 32K
0173 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0174 C.
0175 C. *****
0176 C. TI-CMD SET (OPOG STOP/COPY/START)
0177 C. *****
0178 C.
0179 C. NOTICE ;§ OPOG UPLOAD²-Á÷¿@NG²î¼î¹ç;ç°E²¼òîTI-CMDÁ÷¿@²î¼Á¹Ôª°¬E²ò³òE;f
0180 C. ²²ò¿;çSET²EEDUMP²îÆ±°îYÑY¹ç¹Ôª|²³òE;f
0181 C.
0182 C. TIY³Y²YóYÉòðÁDî¿(UT)
0183 +. TI 2013-01-03 09:09:00.0
0184 DC 01-B3 DHU_OP_STOP
0185 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0186 C.
0187 +. TI 2013-01-03 09:09:01.0
0188 DC 01-B4 DHU_OP_COPY
0189 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0190 C.
0191 +. TI 2013-01-03 09:09:01.0
0192 DC 01-B5 DHU_OPOG_COPY
0193 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP

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0194 C.
0195 +. TI 2013-01-03 09:13:59.5
0196 DC 01-B2 DHU_OP_START
0197 C.      çç[HK1_TI_CMD_NUM]           EQ      1COUNTUP
0198 C.
0199 C.      °È²¼ïÄë%ïíñïîŷÄŷ§ŷÄŷ¹àüŷ
0200 C.      çç[HK1_TI_CMD_ENA/DIS]       EQ      ENA
0201 C.      çç[HK1_TI_CMD_NUM]           EQ      4
0202 C.      çç[HK1_NEXT_EXEC_PIM]        EQ      DHU
0203 C.      çç[HK1_NEXT_EXEC_DC]         EQ      0xB3
0204 C.
0205 C.      *****
0206 C.      TIíŷ°èŷÄŷÖŷ×
0207 C.      *****
0208 C.
0209 C.      TI_TBL(0x03AB00-0x03AEFF;§ 1024byte)
0210 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0211 BC      (03 ab 03 01 02)
0212 C.      çç[HK1_DMP_TOP_ADRS_1]       EQ      07
0213 C.      çç[HK1_DMP_TOP_ADRS_0]       EQ      2B
0214 C.      çç[HK1_DMP_BLOCK_NUM]        EQ      3
0215 C.      çç[HK1_DMP_REPEAT_NUM]       EQ      0
0216 C.      çç[HK1_DMA_DMP_PIM]          EQ      DHU
0217 +. DC 01-22 DHU_MODE_CHNG
0218 BC      (07 0b f8)
0219 C.      çç[HK1_PKT_FORM_NO]          EQ      7
0220 C.      çç[HK1_PKT_GEN_TIME]         EQ      0.25 s
0221 C.      çç[HK1_S_TLM_BIT_RATE]      EQ      32k
0222 C.      çç[HK1_X_TLM_BIT_RATE]      EQ      4M
0223 C.      çç[HK1_DMP_CHK_FLG]         EQ      EXEC
0224 C.
0225 C.      ŷÄŷÖŷ×½ªî»ò³îç§
0226 C.      çç[HK1_DMP_CHK_FLG]          EQ      NON
0227 C.
0228 C.      RAM ID=TI_TBLñîŷÈ¹ç•è²îOKò³îç§
0229 C.
0230 C.      DHUŷâ;¼ŷÈ;È¼ŷ½. ŷî;¼ŷÈ;Èòðîáñ¹
0231 +. DC 01-22 DHU_MODE_CHNG
0232 BC      (02 0a f8)
0233 C.      çç[HK1_PKT_FORM_NO]          EQ      2
0234 C.      çç[HK1_PKT_GEN_TIME]         EQ      0.5S
0235 C.      çç[HK1_S_TLM_BIT_RATE]      EQ      32K
0236 C.      çç[HK1_X_TLM_BIT_RATE]      EQ      4M
0237 C.
0238 C.      *****
0239 C.      SOT TI command set
0240 C.      *****
0241 C.      Execute, after the success of OP upload.
0242 +. TI 2013-01-03 09:13:16.0
0243 DC 07-F0 MDP_SOT_MODE_STBY
0244 BC      (41)
0245 C.      -----
0246 C.      HK1_TI_CMD_NUM      = 1 CNTUP [ ]
0247 C.      -----
0248 C.      ***** SOT END *****
0249 C.      Stop EIS observation and temporarily disable EIS mode changes
0250 C.
0251 C.
0252 C.      ***** Start EIS operation (TI set) *****
0253 C.      Execute, after the success of OP upload.
0254 C.      Set EIS TI-commands
0255 +. TI 2013-01-03 09:13:30.0
0256 DC 07-FC EIS_MODE_MANU
0257 BC      (21 02)
0258 +. TI 2013-01-03 09:13:40.0
0259 DC 07-FC EIS_MODE_CHG_DIS
0260 BC      (22)
0261 C.      [ ] [HK1_TI_CMD_NUM]         EQ      2 COUNTUP
0262 C.      ***** End EIS operation (TI set) *****
0263 C.
0264 C.
0265 C.
0266 C.      ***** XRT START *****
0267 C.      Execute, after the success of OP upload.
0268 +. TI 2013-01-03 09:13:00.0
0269 DC 07-F0 MDP_XRT_MODE_STBY
0270 BC      (c3)
0271 C.      [ ] [HK1_TI_CMD_NUM]         EQ      1COUNTUP
0272 C.
0273 C.      ***** XRT END *****
0274 C.
0275 C.      ***** MDP ´ûÄîñî»ö¼ŷñÈÄðñ¹ñèDCBC•x²è *****
0276 C.      (¼á°îŷÖŷÄŷÈŷŷŷÈŷáŷçŷèèÈ¼òñ¼Ä»Ûñ¹ñè)
0277 C.      S. DC-BC dcbc-402:DCBC
0278 C.      (MDP_known_event)
0279 C.
0280 C.
0281 C.      ***** ŷĐŷ¹•İ Daily±çîññÈ´Øñ¹ñèDCBC•x²è *****
0282 C.      S. DC-BC dcbc-153:DCBC
0283 C.      (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0284 C.
0285 C.
0286 C.      ;ãLOSŷÄŷ§ŷÄŷ¹¼Ä»Û;ã
0287 C.
0288 C.      ***** LOS *****
0289 C.

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(a) Spacecraft Operation Procedure (real-commands)

```
main-368 2013-01-03 13:46:40 271 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. ;ãAOSYÁYŞYÁY-¼Á»Û;ã
0005 C.
0006 C. YÀYß;¼Y³YËYÓYÉÁ+ç®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCs : Reload orbital element (send every contact) *****
0010 C. Áí;ËçµÁµ°µ»í×ÁÇçíYçYÁY×Yí;¼YÉ;ËÈèµ°ííÉ;ÈµÈ¼°ÇÇµ°µç¼í¹çµí;çÀ®, ùµ¹µèµµçÇÁ+ç®µ°µÈµµµ³µÈ;f
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 . C. *****
0015 C. XÁ+çµ;ON
0016 C. *****
0017 C. ç" °ÆÀ, í×ÈYµäLOSµµçµí»p´Öµð¹íí, µ.; çÉÖí×µÈXÁÓONµí¹ÔµÈµíµÈµµ³µÈ;f
0018 C.
0019 +. DC 03-B4 TCIA_XPA_ON/HI
0020 M. WAIT_SEC 1
0021 + DC 03-84 TCIA_XMOD_ON
0022 M. WAIT_SEC 1
0023 + DC 03-95 TCIA_XMOD_QPSK
0024 C. çç[HK1_XPA_ON/OFF] EQ ON
0025 C. çç[HK1_XPA_PWR_HI/LO] EQ HI
0026 C. çç[HK1_XMOD_ON/OFF] EQ ON
0027 C. çç[HK1_XMOD_QPSK/PM] EQ QPSK
0028 C.
0029 . C. XYDYÓYÉYíYÁY-¾ÔÁÖµ°µçµé; ç°È²¼µí°ÆÀ, ¼È¼çµð¼Á¹Ôµ¹µé;f
0030 C.
0031 . C. *****
0032 C. DR PT1 Áí¼í°ÆÀ,
0033 C. *****
0034 C. ç" RESTART;ÈPT1;Èµ°µçµ¼¼í¹çµí; ç°È²¼µí°ÆÀ¹Ôµ»µ°; çDCBC-150µØçÈµà;f
0035 C.
0036 . C. ;ãPT1°ÆÀ, ³«»í;ã
0037 +. DC 01-29 DHU_S/X_VC4_OFF
0038 + DC 06-C8 DR_PT1_REP_SEL
0039 BC (01 00)
0040 + DC 06-B3 DR_REP_START
0041 + DC 01-32 DHU_X_VC4_ON
0042 C. çç[HK1_REP_PT_1/2] EQ PT1 (¼Á¹Ô, ;¼Ú)
0043 C. çç[HK1_REP_STA/STP] EQ START (¼Á¹Ô, ;¼Ú)
0044 C. çç[HK1_X_VC4_ON/OFF] EQ ON (¼Á¹Ô, ;¼Ú)
0045 C.
0046 . C. ;ãYçYÓYÉYÈÁÚÁØ;ÈÁ°Á°²óÈð;È, áµí°ÆÀ, °Æ³«;ã
0047 +. DC 06-B3 DR_REP_START
0048 + DC 01-32 DHU_X_VC4_ON
0049 C. çç[HK1_REP_PT_1/2] EQ PT1 (¼Á¹Ô, ;¼Ú)
0050 C. çç[HK1_REP_STA/STP] EQ START (¼Á¹Ô, ;¼Ú)
0051 C. çç[HK1_X_VC4_ON/OFF] EQ ON (¼Á¹Ô, ;¼Ú)
0052 C.
0053 C.
0054 . C. PT1°ÆÀ, µ-¼«Æ°Áá»ßµ°µçµ, á; ç°È²¼µð¼Á¹Ôµ¹µé;f
0055 C. YçYÓYÉYÈÁÚÁØµáÁ°Á°²óÈðµ-µáµ¼¼í¹çµí°°í»µ¹µèµµçÇÁÓµÀ;f
0056 C.
0057 . C. *****
0058 C. DR PT2 Áí¼í°ÆÀ,
0059 C. *****
0060 C. ç" RESTART;ÈPT2;Èµ°µçµ¼¼í¹çµí; ç°È²¼µí°ÆÀ¹Ôµ»µ°; çDCBC-151µØçÈµà;f
0061 C.
0062 . C. ;ãPT2°ÆÀ, ³«»í;ã
0063 +. DC 01-29 DHU_S/X_VC4_OFF
0064 + DC 06-C8 DR_PT2_REP_SEL
0065 BC (02 00)
0066 + DC 06-B3 DR_REP_START
0067 + DC 01-32 DHU_X_VC4_ON
0068 C. çç[HK1_REP_PT_1/2] EQ PT2 (¼Á¹Ô, ;¼Ú)
0069 C. çç[HK1_REP_STA/STP] EQ START (¼Á¹Ô, ;¼Ú)
0070 C. çç[HK1_X_VC4_ON/OFF] EQ ON (¼Á¹Ô, ;¼Ú)
0071 C.
0072 . C. ;ãYçYÓYÉYÈÁÚÁØ;ÈÁ°Á°²óÈð;È, áµí°ÆÀ, °Æ³«;ã
0073 +. DC 06-B3 DR_REP_START
0074 + DC 01-32 DHU_X_VC4_ON
0075 C. çç[HK1_REP_PT_1/2] EQ PT2 (¼Á¹Ô, ;¼Ú)
0076 C. çç[HK1_REP_STA/STP] EQ START (¼Á¹Ô, ;¼Ú)
0077 C. çç[HK1_X_VC4_ON/OFF] EQ ON (¼Á¹Ô, ;¼Ú)
0078 C.
0079 . C. *****
0080 C. DR°ÆÀ, Áá»ß;çXÁ+çµ;OFF
0081 C. *****
0082 C.
0083 . C. ;ãDR°ÆÀ, Áá»ß;ã
0084 +. DC 06-B4 DR_REP_STOP
0085 + DC 01-29 DHU_S/X_VC4_OFF
0086 C. çç[HK1_REP_STA/STP] EQ STOP
0087 C. çç[HK1_S_VC4_ON/OFF] EQ OFF
0088 C. çç[HK1_X_VC4_ON/OFF] EQ OFF
0089 C.
0090 . C. ;ãXÁ+çµ;OFF;ã
0091 +. DC 03-85 TCIA_XMOD_OFF
0092 M. WAIT_SEC 1
0093 + DC 03-B5 TCIA_XPA_OFF
0094 C. çç[HK1_XMOD_ON/OFF] EQ OFF
0095 C. çç[HK1_XPA_ON/OFF] EQ OFF
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0096 C.
0097 C.
0098 C.
0099 C. ***** XRT START *****
0100 C.
0101 +. DC 07-F0 MDP_XRT_CTRL_MANU
0102 BC (c1)
0103 + DC 07-F0 MDP_XRT_MODE_STBY
0104 BC (c3)
0105 . C. ----- Success Verify ? OK / NG ____
0106 C.
0107 C. XRT Obs. Table Upload
0108 . S. RAM ram-291:MDP_OBS_X
0109 ( )
0110 C.
0111 +. DC 07-F0 MDP_DUMP_XRTTBL
0112 BC (84 07 00 00 00 3a d4)
0113 . C. ----- Comparison Check ? OK / ERR ____
0114 C.
0115 C.
0116 +. DC 07-F0 MDP_XRT_ROI_SET
0117 BC (cd 01 b1 b1 04 04)
0118 + DC 07-F0 MDP_XRT_ROI_SET
0119 BC (cd 02 b1 b1 08 08)
0120 + DC 07-F0 MDP_XRT_ROI_SET
0121 BC (cd 03 b1 b1 08 08)
0122 + DC 07-F0 MDP_XRT_ROI_SET
0123 BC (cd 04 b1 b1 06 06)
0124 + DC 07-F0 MDP_XRT_ROI_SET
0125 BC (cd 05 85 83 06 06)
0126 + DC 07-F0 MDP_XRT_ROI_SET
0127 BC (cd 06 85 83 06 06)
0128 + DC 07-F0 MDP_XRT_ROI_SET
0129 BC (cd 07 85 83 08 08)
0130 + DC 07-F0 MDP_XRT_ROI_SET
0131 BC (cd 08 80 80 20 20)
0132 + DC 07-F0 MDP_XRT_ROI_SET
0133 BC (cd 09 80 80 20 08)
0134 + DC 07-F0 MDP_XRT_ROI_SET
0135 BC (cd 0a 80 80 08 20)
0136 + DC 07-F0 MDP_XRT_ROI_SET
0137 BC (cd 0f 80 80 06 06)
0138 + DC 07-F0 MDP_XRT_ROI_SET
0139 BC (cd 10 80 80 08 08)
0140 + DC 07-F0 MDP_XRT_FLD_ENA
0141 BC (d8)
0142 + DC 07-F0 MDP_XRT_FLRCTRL_ENA
0143 BC (c8)
0144 + DC 07-F0 MDP_XRT_AEC_RESET
0145 BC (d0)
0146 + DC 07-F0 MDP_XRT_ARS_DIS
0147 BC (d5)
0148 + DC 07-F0 MDP_XRT_FLD_RESET
0149 BC (da)
0150 + DC 07-F0 MDP_XRT_QT_PROG_SET
0151 BC (c4 03)
0152 +. DC 07-F0 MDP_XRT_FL_PROG_SET
0153 BC (c5 10)
0154 . C. ----- Success Verify ? OK / NG ____
0155 C.
0156 C.
0157 . C. All OK? Yes--> Please Proceed. / No --> Stop here.
0158 C.
0159 +. DC 07-F0 MDP_XRT_MODE_OBSV
0160 BC (c2)
0161 +. TI 2013-01-03 09:13:02.0
0162 DC 07-F0 MDP_XRT_MODE_OBSV
0163 BC (c2)
0164 . C. ----- Success Verify ? OK / NG ____
0165 C.
0166 C. ***** XRT END *****
0167 . C. *****
0168 C. SOT table upload
0169 C. *****
0170 . C. < Stop FG table >
0171 +. DC 07-F0 MDP_FG_CTRL_MANU
0172 BC (51)
0173 . C. -----
0174 C. MDP_FG_CTRL_MODE = MANU [ ]
0175 C. -----
0176 C.
0177 . C. <Upload FG Observation Table>
0178 . S. RAM ram-262:MDP_OBS_F
0179 ( )
0180 C.
0181 . C. < Dump RAMID=MDP_OBS_F >
0182 +. DC 07-F0 MDP_DUMP_FGTBL
0183 BC (82 07 00 00 00 38 b8)
0184 C. -----
0185 C. MDP_OBS_F verify = OK/NG [ ]
0186 C. -----
0187 C.
0188 . C. < Stop SP table >
0189 +. DC 07-F0 MDP_SP_CTRL_MANU
0190 BC (61)
0191 C. -----
0192 C. MDP_SP_CTRL_MODE = MANU [ ]
0193 C. -----

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0194 C.
0195 . C. <Upload SP Observation Table>
0196 . S. RAM ram-285:MDP_OBS_S
0197 ( )
0198 C.
0199 . C. < Dump RAMID=MDP_OBS_S >
0200 +. DC 07-F0 MDP_DUMP_SPTBL
0201 BC (83 07 00 00 00 38 b8)
0202 C. -----
0203 C. MDP_OBS_S verify = OK/NG [ ]
0204 C. -----
0205 C.
0206 . C. < Upload DPL table >
0207 C.
0208 C. MDP_OBS_S verify = OK/NG [ ]
0209 C.
0210 . S. RAM ram-271:MDP_DPL
0211 ( )
0212 C.
0213 . C. < Dump RAMID=MDP_DPL >
0214 +. DC 07-F0 MDP_DUMP_FGTBL
0215 BC (82 07 00 38 b8 00 40)
0216 C. -----
0217 C. MDP_DPL verify = OK [ ]
0218 C. -----
0219 C.
0220 C. STS_CHK ON [ ]
0221 C.
0222 . C. < Update MDP DSC PAR1 >
0223 +. DC 07-F0 MDP_DSC_PAR1_UPDATE
0224 BC (4c)
0225 C. MDP_CMD_CODE = F04C0700 [ ]
0226 C. MDP_CMD_CNT (count-up 1) [ ]
0227 C. -----
0228 C.
0229 . C.
0230 . C. < Resume FG table (auto mode) >
0231 +. DC 07-F0 MDP_FG_CTRL_AUTO
0232 BC (50)
0233 C. -----
0234 C. MDP_FG_CTRL_MODE = AUTO [ ]
0235 C. -----
0236 C.
0237 C. *****
0238 C. SOT TI command set
0239 C. *****
0240 C. Execute, after the success of TBL upload.
0241 +. TI 2013-01-03 09:13:18.0
0242 DC 07-F0 MDP_SOT_MODE_OBSV
0243 BC (40)
0244 C. -----
0245 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0246 C. -----
0247 C.
0248 C. Only when FG_CTRL_AUTO is used in RT.
0249 +. TI 2013-01-03 09:13:20.0
0250 DC 07-F0 MDP_FG_CTRL_AUTO
0251 BC (50)
0252 C. -----
0253 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0254 C. -----
0255 C. ***** SOT END *****
0256 C.
0257 C. ***** MDP 'uãîï»ö%ýñÊð¹ñèDCBC•x²è *****
0258 C. (%ã°îÿÓÿÄÿÈÿËÿÏÿÑÿÛÿÝÿßÿàÿâÿäÿæÿèÿêÿìÿîÿðÿñÿÿ»Û¹ñè)
0259 . S. DC-BC dcbc-402:DCBC
0260 (MDP_known_event)
0261 C.
0262 C.
0263 . C. ***** MDP 'uãîï»ö%ýñÊð¹ñèDCBC•x²è *****
0264 . S. DC-BC dcbc-153:DCBC
0265 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0266 C.
0267 C.
0268 . C. ÿãLOSÿÁÿ$ÿÄÿ-¼Â»Û;ä
0269 C.
0270 . C. ***** LOS *****
0271 C.

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Jan 03, 13 13:47

## XRT\_OGLIST\_0156.chk

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\*\*\* OP Sequence for XRT \*\*\*

2013/01/03	09:24:00.0	AOCS_OrE-point_Start_1_OG [0x097]							
		AOCU_NM	5	02-76	04	00	00	00	00
2013/01/04	09:23:00.0	XRT_CTRL_MANU_402_OG [0x192]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	09:23:02.0	XRT_FOCUS_POSITION_420_OG [0x1a4]							
		XRT_FOCUS_POSITION	4	07-F8	22	fe	97	00	
2013/01/04	09:23:22.0	XRT_FLD_ENA_428_OG [0x1ac]							
		MDP_XRT_FLD_ENA	1	07-F0	d8				
2013/01/04	09:23:24.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]							
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8				
2013/01/04	09:23:26.0	XRT_AEC_RESET_423_OG [0x1a7]							
		MDP_XRT_AEC_RESET	1	07-F0	d0				
2013/01/04	09:23:28.0	XRT_ARS_DIS_438_OG [0x1b6]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/04	09:23:30.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/04	09:23:32.0	XRT_QT_PROG_SET_439_OG [0x1b7]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4	13			
2013/01/04	09:23:34.0	XRT_FL_PROG_SET_444_OG [0x1bc]							
		MDP_XRT_FL_PROG_SET	2	07-F0	c5	10			
2013/01/04	09:23:36.0	XRT_CTRL_AUTO_408_OG [0x198]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/04	10:01:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	10:01:02.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/04	10:01:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/04	10:04:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/04	10:13:30.5	XRT_Custom_434_OG [0x1b2]							
2013/01/04	10:14:30.5	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/04	14:40:00.0	XRT_CTRL_MANU_402_OG [0x192]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	14:40:02.0	XRT_FOCUS_POSITION_420_OG [0x1a4]							
		XRT_FOCUS_POSITION	4	07-F8	22	fe	97	00	
2013/01/04	14:40:22.0	XRT_FLD_ENA_428_OG [0x1ac]							
		MDP_XRT_FLD_ENA	1	07-F0	d8				
2013/01/04	14:40:24.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]							
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8				
2013/01/04	14:40:26.0	XRT_AEC_RESET_423_OG [0x1a7]							
		MDP_XRT_AEC_RESET	1	07-F0	d0				
2013/01/04	14:40:28.0	XRT_ARS_DIS_437_OG [0x1b5]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/04	14:43:00.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/04	14:43:02.0	XRT_QT_PROG_SET_436_OG [0x1b4]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4	0a			
2013/01/04	14:43:04.0	XRT_FL_PROG_SET_444_OG [0x1bc]							
		MDP_XRT_FL_PROG_SET	2	07-F0	c5	10			
2013/01/04	14:43:06.0	XRT_CTRL_AUTO_408_OG [0x198]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/04	15:24:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	15:24:02.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/04	15:24:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/04	15:27:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/04	15:47:00.0	XRT_Custom_434_OG [0x1b2]							
2013/01/04	15:48:00.0	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/04	17:00:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	17:00:02.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/04	17:00:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/04	17:03:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/04	17:24:00.0	XRT_Custom_434_OG [0x1b2]							
2013/01/04	17:25:00.0	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/04	17:59:54.0	XRT_CTRL_MANU_402_OG [0x192]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/04	17:59:56.0	XRT_FOCUS_RECALIBRATE_425_OG [0x1a9]							
		XRT_FOCUS_RECAL	2	07-F8	78	00			
2013/01/04	18:00:00.0	AOCS_OrE-point_Start_2_OG [0x098]							
		AOCU_NM	5	02-76	00	00	00	00	00
2013/01/04	18:03:56.0	XRT_FOCUS_POSITION_403_OG [0x193]							
		XRT_FOCUS_POSITION	4	07-F8	22	ff	aa	00	
2013/01/04	18:04:16.0	XRT_FLD_DIS_404_OG [0x194]							
		MDP_XRT_FLD_DIS	1	07-F0	d9				
2013/01/04	18:04:18.0	XRT_FLRCTRL_DIS_405_OG [0x195]							
		MDP_XRT_FLRCTRL_DIS	1	07-F0	c9				
2013/01/04	18:04:20.0	XRT_ARS_DIS_412_OG [0x19c]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/04	18:04:22.0	XRT_QT_PROG_SET_419_OG [0x1a3]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4	0d			

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2013/01/04	18:04:24.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/04	18:09:54.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/04	18:09:56.0	XRT_FOCUS_POSITION_420_OG [0x1a4]			
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2013/01/04	18:10:00.0	AOCS_OrE-point_Start_1_OG [0x097]			
		AOCU_NM	5	02-76	04 00 00 00 00
2013/01/04	18:10:16.0	XRT_FLD_ENA_428_OG [0x1ac]			
		MDP_XRT_FLD_ENA	1	07-F0	d8
2013/01/04	18:10:18.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]			
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2013/01/04	18:10:20.0	XRT_AEC_RESET_423_OG [0x1a7]			
		MDP_XRT_AEC_RESET	1	07-F0	d0
2013/01/04	18:10:22.0	XRT_ARS_DIS_437_OG [0x1b5]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/04	18:12:54.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/04	18:12:56.0	XRT_QT_PROG_SET_436_OG [0x1b4]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0a
2013/01/04	18:12:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]			
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 10
2013/01/04	18:13:00.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/04	18:37:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/04	18:37:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/04	18:37:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/04	18:40:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/04	19:00:30.0	XRT_Custom_434_OG [0x1b2]			
2013/01/04	19:01:30.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/04	20:14:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/04	20:14:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/04	20:14:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/04	20:17:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/04	20:38:00.0	XRT_Custom_434_OG [0x1b2]			
2013/01/04	20:39:00.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/04	21:52:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/04	21:52:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/04	21:52:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/04	21:55:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/04	22:14:00.0	XRT_Custom_434_OG [0x1b2]			
2013/01/04	22:15:00.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/04	23:29:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/04	23:29:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/04	23:29:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/04	23:32:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/04	23:41:00.0	XRT_Custom_434_OG [0x1b2]			
2013/01/04	23:42:00.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/05	00:57:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/05	00:57:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/05	00:57:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/05	01:00:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/05	01:12:30.0	XRT_Custom_434_OG [0x1b2]			
2013/01/05	01:13:30.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/05	02:28:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/05	02:28:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/05	02:28:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/05	02:31:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/05	02:49:00.5	XRT_Custom_434_OG [0x1b2]			
2013/01/05	02:50:00.5	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/05	03:57:00.5	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/05	03:57:02.5	XRT_FLD_RESET_424_OG [0x1a8]			

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2013/01/05	03:57:04.5	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_FLD_RESET	1	07-F0	da		
			MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/05	04:00:14.5	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/05	04:26:30.0	XRT_Custom_434_OG [0x1b2]						
2013/01/05	04:27:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	05:37:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	05:37:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/05	05:37:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/05	05:40:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/05	06:04:00.5	XRT_Custom_434_OG [0x1b2]						
2013/01/05	06:05:00.5	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	06:13:54.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	06:13:56.0	XRT_FOCUS_POSITION_403_OG [0x193]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00		
2013/01/05	06:14:00.0	AOCS_Ore-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	00 00 00 00 00		
2013/01/05	06:14:16.0	XRT_FLD_DIS_404_OG [0x194]	MDP_XRT_FLD_DIS	1	07-F0	d9		
2013/01/05	06:14:18.0	XRT_FLRCTRL_DIS_405_OG [0x195]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9		
2013/01/05	06:14:20.0	XRT_ARS_DIS_406_OG [0x196]	MDP_XRT_ARS_DIS	1	07-F0	d5		
2013/01/05	06:16:58.0	XRT_QT_PROG_SET_419_OG [0x1a3]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d		
2013/01/05	06:17:00.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	06:23:54.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	06:23:56.0	XRT_FOCUS_POSITION_420_OG [0x1a4]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00		
2013/01/05	06:24:00.0	AOCS_Ore-point_Start_1_OG [0x097]	AOCU_NM	5	02-76	04 00 00 00 00		
2013/01/05	06:24:16.0	XRT_FLD_ENA_428_OG [0x1ac]	MDP_XRT_FLD_ENA	1	07-F0	d8		
2013/01/05	06:24:18.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8		
2013/01/05	06:24:20.0	XRT_AEC_RESET_423_OG [0x1a7]	MDP_XRT_AEC_RESET	1	07-F0	d0		
2013/01/05	06:24:22.0	XRT_ARS_DIS_437_OG [0x1b5]	MDP_XRT_ARS_DIS	1	07-F0	d5		
2013/01/05	06:26:54.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/05	06:26:56.0	XRT_QT_PROG_SET_436_OG [0x1b4]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 0a		
2013/01/05	06:26:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 10		
2013/01/05	06:27:00.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	07:18:00.5	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	07:18:02.5	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/05	07:18:04.5	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/05	07:21:14.5	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/05	07:41:30.0	XRT_Custom_434_OG [0x1b2]						
2013/01/05	07:42:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	08:57:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	08:57:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/05	08:57:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/05	09:00:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/05	09:17:00.0	XRT_Custom_434_OG [0x1b2]						
2013/01/05	09:18:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/05	10:30:00.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/05	11:11:00.0	AOCS_Ore-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	00 00 00 00 00		