

XRT Timeline to be uploaded on 2013/01/10

Period: 2013/01/10 10:50:00 - 2013/01/15 10:39:00

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Normal mode

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XOB #190F: HOP81 2-filter - Ti/poly 8s, Al/mesh 4s, G-band - 384x384 45ms													
Term	Pointing (x, y)					Comment							
01/10 11:03:00 - 01/10 16:59:54	Fixed (-15.0, 883.0)					# OP start + 10min, HOP 81, polar monitoring, N pole.							
PROG= 15 Inf.-time(s)													
└─ Subr= 1 1-time(s) 2.0sec													
└─ Seqn= 61 2-time(s) 2.0sec													
└─ Open/G-band Open/G-band close Safe Norm 63ms Obs 1x1 512x512 (1064, 1048) DPCM 0 0 2.0sec													
└─ Subr= 2 1-time(s) 2.0sec													
└─ Seqn= 62 1-time(s) 30.0sec													
└─ Open/G-band Open/G-band open Safe Norm 44ms Obs 1x1 384x384 (1064, 1048) Q=90 0 0 2.0sec													
└─ Subr= 3 30-time(s) 2.0sec													
└─ Seqn= 60 2-time(s) 30.0sec													
└─ Open/Al-mesh Open/Al-mesh close Safe Norm 4.00s Obs 1x1 384x384 (1064, 1048) Q=90 0 0 2.0sec													
└─ Open/Ti-poly Open/Ti-poly close Safe Norm 4.00s Obs 1x1 384x384 (1064, 1048) Q=90 0 0 2.0sec													
Default Filter Thicker Filter VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval													

XOB #195F: AR Standard-B(Morphology) with PFB, thin-Be + multifilter context, 384x384 at 1064 1048, 60s-cad, shorter G-band (32ms) w/ G-Band VLS Clo													
Term	Pointing (x, y)					Comment							
01/10 17:03:00 - 01/10 18:05:54	Track (-310.4, 388.4) @ 01/10 17:00:00					* Track AR 11652							
01/10 18:19:00 - 01/11 05:36:24	Track (-299.9, 388.7) @ 01/10 18:16:00					# Track AR 11652							
01/11 05:49:30 - 01/11 17:39:24	Track (-202.8, 391.5) @ 01/11 05:46:30					# Cont.							
PROG= 18 Inf.-time(s)													
└─ Subr= 1 1-time(s) 2.0sec													
└─ Seqn=100 1-time(s) 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 16.0s Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec													
└─ Open/G-band Open/G-band open Safe Norm 32ms Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec													
└─ Seqn= 19 1-time(s) 2.0sec													
└─ Open/G-band Open/G-band close Safe Norm 63ms Obs 1x1 384x384 (1064, 1048) DPCM 0 0 2.0sec													
└─ Seqn= 65 4-time(s) 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ Open/thick-Al Open/thick-Al close Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ Al-poly/Open Al-poly/thick-Be close Safe Norm 250ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ C-poly/Open C-poly/thick-Al close Safe Norm 250ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ thin-Be/Open med-Be/Open close Safe Norm 1.00s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ med-Be/Open med-Be/Open close Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ med-Al/Open med-Al/thick-Al close Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec													
└─ Subr= 2 1-time(s) 2.0sec													
└─ Seqn= 94 70-time(s) 2.0sec													
└─ thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 15.0sec													
└─ thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 15.0sec													
└─ thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 15.0sec													
└─ thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 3 15.0sec													
Default Filter Thicker Filter VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval													

XOB #192F: Synoptic Q95 2x2 - Al/mesh(33/1024) + Dark cal(2x2 4x4 8x8 512 Q98) + Dark cal(1x1 512x2048 -1x1 2048x512) + Ti-poly(64/1443) + Thin-Be(18													
Term	Pointing (x, y)					Comment							
01/10 18:09:00 - 01/10 18:15:54	Fixed (0.0, 0.0)					synoptic, shifted 6.0 min							
01/11 05:39:30 - 01/11 05:46:24	Fixed (0.0, 0.0)					synoptic, shifted -23.5 min							
01/11 17:42:30 - 01/11 17:49:24	Fixed (0.0, 0.0)					synoptic, shifted -20.5 min							
01/12 06:01:00 - 01/12 06:07:54	Fixed (0.0, 0.0)					synoptic, shifted -2.0 min							
PROG= 13 1-time(s)													
└─ Subr= 1 1-time(s) 14.0sec													
└─ Seqn= 64 1-time(s) 4.0sec													
└─ Open/Al-mesh Open/Ti-poly close Safe Norm 32ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Open/Al-mesh Open/Ti-poly close Safe Norm 1.00s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Seqn= 6 1-time(s) 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 2x2 2048x2048 (1024, 1024) Q=98 0 0 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 4x4 2048x2048 (1024, 1024) Q=98 0 0 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 8x8 2048x2048 (1024, 1024) Q=98 0 0 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 1x1 2048x512 (1024, 1024) DPCM 0 0 2.0sec													
└─ Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 1x1 512x2048 (1024, 1024) DPCM 0 0 2.0sec													
└─ Seqn= 70 1-time(s) 4.0sec													
└─ Open/Ti-poly Open/Ti-poly close Safe Norm 63ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Open/Ti-poly Open/Ti-poly close Safe Norm 1.41s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Seqn= 67 1-time(s) 2.0sec													
└─ thin-Be/Open thin-Be/Open close Safe Norm 177ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ thin-Be/Open thin-Be/Open close Safe Norm 2.83s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Seqn= 69 1-time(s) 2.0sec													
└─ Open/G-band Open/G-band open Safe Norm 8ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec													
└─ Subr= 2 1-time(s) 2.0sec													
└─ Seqn= 68 1-time(s) 2.0sec													
└─ Open/G-band Open/G-band close Safe Norm 32ms Obs 1x1 2048x2048 (1024, 1024) DPCM 0 0 2.0sec													

Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)	Comp.	AEC Buffer	Interval
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XOB #1962: AR Standard-B(Morphology) with PFB, thin-Be + multifilter context, 384x384 at 1064 1048, 120s-cad, shorter G-band (33ms) w/ G-Band VLS Cl

Term	Pointing (x, y)	Comment
01/11 17:52:30 - 01/12 05:57:54	Track (-98.5, 393.6) @ 01/11 17:49:30	# Cont.
01/12 06:11:00 - 01/12 09:50:00	Track (9.4, 394.9) @ 01/12 06:08:00	# Cont.
PROG= 07 Inf.-time(s)		
Subr= 1 1-time(s) 2.0sec		
Seqn=100 1-time(s) 2.0sec		
Open/Ti-poly	Open/thick-Al close	Safe Dark 16.0s Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
Open/G-band	Open/G-band open	Safe Norm 32ms Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
Seqn= 19 1-time(s) 2.0sec		
Open/G-band	Open/G-band close	Safe Norm 63ms Obs 1x1 384x384 (1064, 1048) DPCM 0 0 2.0sec
Seqn= 65 4-time(s) 2.0sec		
Open/Ti-poly	Open/thick-Al close	Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
Open/thick-Al	Open/thick-Al close	Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
Al-poly/Open	Al-poly/thick-Be close	Safe Norm 250ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
C-poly/Open	C-poly/thick-Al close	Safe Norm 250ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
thin-Be/Open	med-Be/Open close	Safe Norm 1.00s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
med-Be/Open	med-Be/Open close	Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
med-Al/Open	med-Al/thick-Al close	Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
Subr= 2 1-time(s) 2.0sec		
Seqn= 73 70-time(s) 120.0sec		
thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 12.5sec
thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 12.5sec
thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 12.5sec
thin-Be/Open	med-Be/Open close	Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 3 12.5sec
Default Filter	Thicker Filter	VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

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Flare mode

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XOB #1920: Flare obs. dynamics - thin-Be high cadence + context (med-Al,thick-Be -384x384 + Al-poly 512x512 2x2)-Gband (45ms)-15 loops

Term	Pointing (x, y)	Comment
01/10 11:03:00 - 01/10 16:59:54	Fixed (-15.0, 883.0)	# OP start + 10min, HOP 81, polar monitoring, N pole.
01/10 17:03:00 - 01/10 18:05:54	Track (-310.4, 388.4) @ 01/10 17:00:00	* Track AR 11652
01/10 18:19:00 - 01/11 05:36:24	Track (-299.9, 388.7) @ 01/10 18:16:00	# Track AR 11652
01/11 05:49:30 - 01/11 17:39:24	Track (-202.8, 391.5) @ 01/11 05:46:30	# Cont.
01/11 17:52:30 - 01/12 05:57:54	Track (-98.5, 393.6) @ 01/11 17:49:30	# Cont.
01/12 06:11:00 - 01/12 09:50:00	Track (9.4, 394.9) @ 01/12 06:08:00	# Cont.
PROG= 16 15-time(s)		
Subr= 1 45-time(s) 10.0sec		
Seqn= 35 1-time(s) 2.0sec		
thin-Be/Open	med-Be/Open close	Safe Norm 250ms Obs 1x1 384x384 (1024, 1024) Q=95 3 0 2.0sec
Subr= 2 1-time(s) 10.0sec		
Seqn= 36 1-time(s) 2.0sec		
med-Al/Open	med-Al/thick-Al close	Safe Norm 500ms Obs 1x1 384x384 (1024, 1024) Q=95 3 0 2.0sec
Open/thick-Be	Open/thick-Be close	Safe Norm 2.00s Obs 1x1 384x384 (1024, 1024) Q=95 3 0 2.0sec
Seqn= 37 1-time(s) 2.0sec		
Al-poly/Open	Al-poly/thick-Al close	Safe Norm 125ms Obs 2x2 512x512 (1024, 1024) Q=95 2 0 2.0sec
Seqn= 38 1-time(s) 2.0sec		
Open/G-band	Open/G-band open	Safe Norm 44ms Obs 1x1 384x384 (1024, 1024) Q=98 0 0 2.0sec
Open/thick-Al	Open/thick-Al close	Safe Dark 1.00s Obs 1x1 384x384 (1024, 1024) Q=98 0 0 2.0sec
Open/thick-Al	Open/thick-Al close	Safe Dark 1.00s Obs 2x2 512x512 (1024, 1024) Q=98 0 0 2.0sec
Default Filter	Thicker Filter	VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

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Active Region Search

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NOT USED

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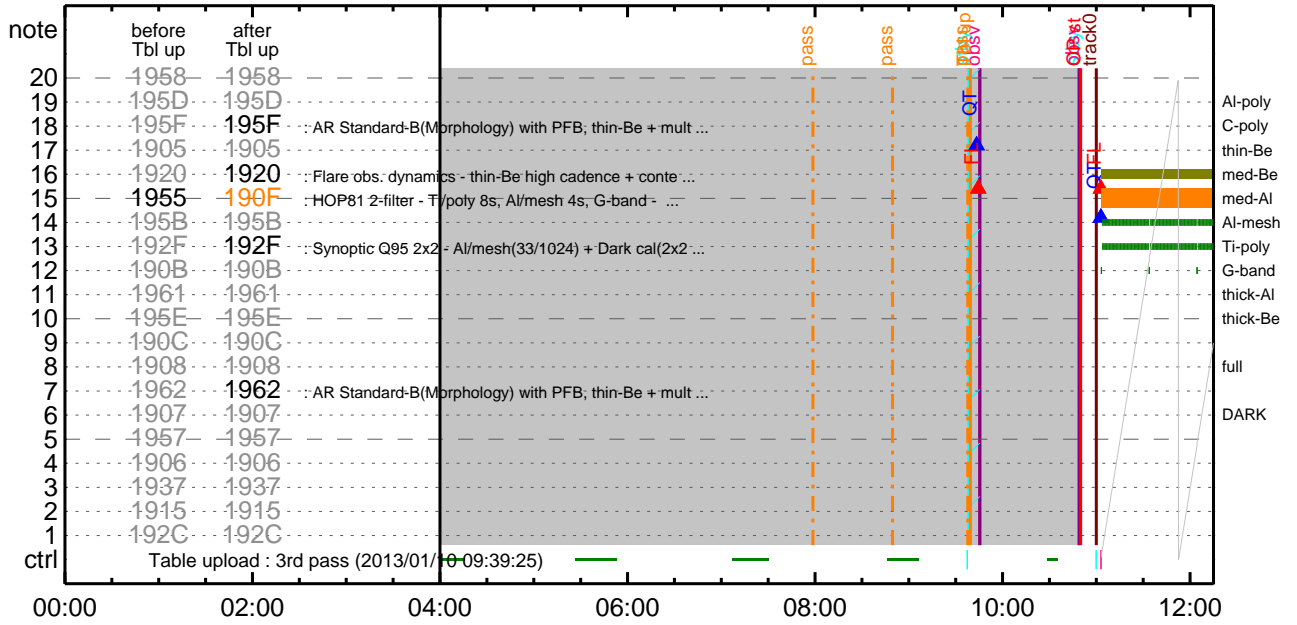
Flare Detection

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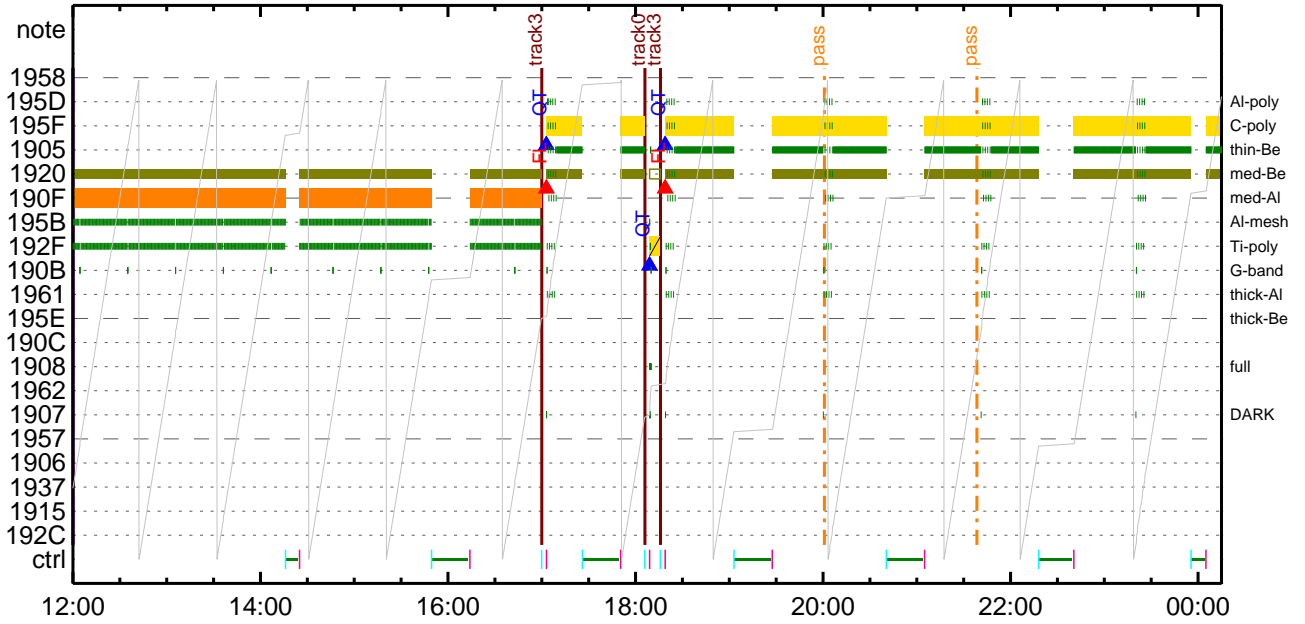
FLD Patrol

Term	Pointing (x, y)	Comment
01/10 18:16:16 - 01/11 05:36:46	Track (-299.9, 388.7) @ 01/10 18:16:00	# Track AR 11652
01/11 05:46:46 - 01/11 17:39:46	Track (-202.8, 391.5) @ 01/11 05:46:30	# Cont.
01/11 17:49:46 - 01/12 05:58:16	Track (-98.5, 393.6) @ 01/11 17:49:30	# Cont.
01/12 06:08:16 - 01/15 10:39:00	Track (9.4, 394.9) @ 01/12 06:08:00	# Cont.
Open/Ti-poly	Open/thick-Al close	Safe Norm 8ms Obs 8x8 Q=50 30sec
Default Filter	Thicker Filter	VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

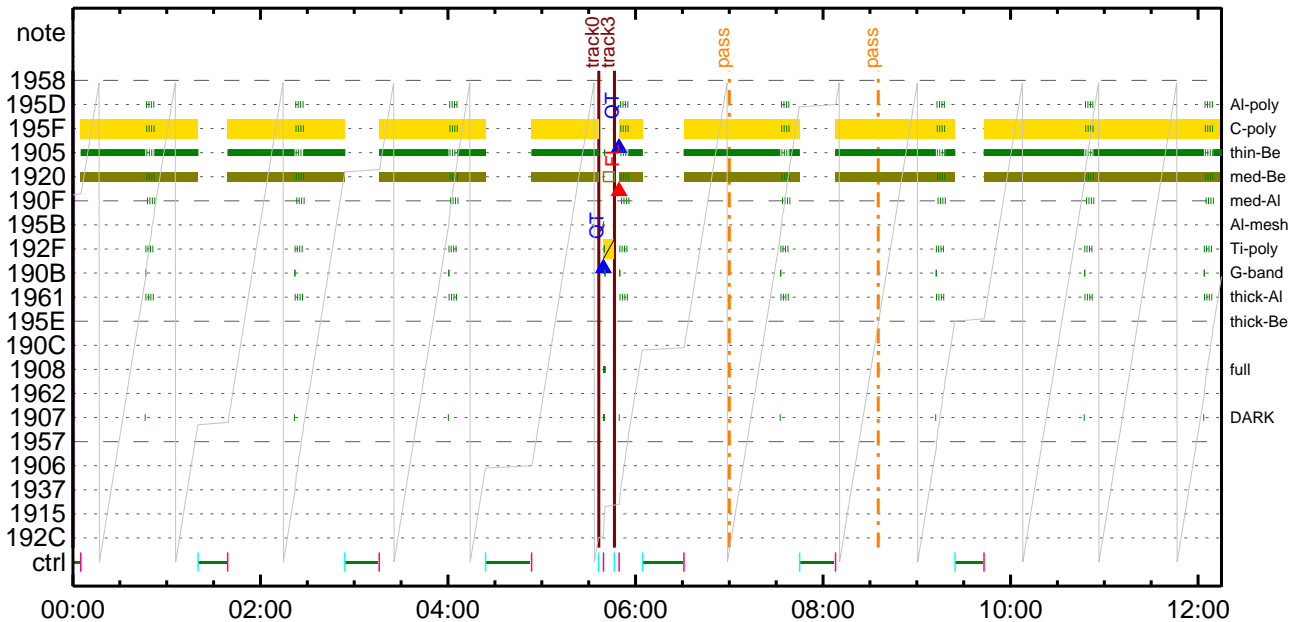
CMDI #0170 2013/01/10



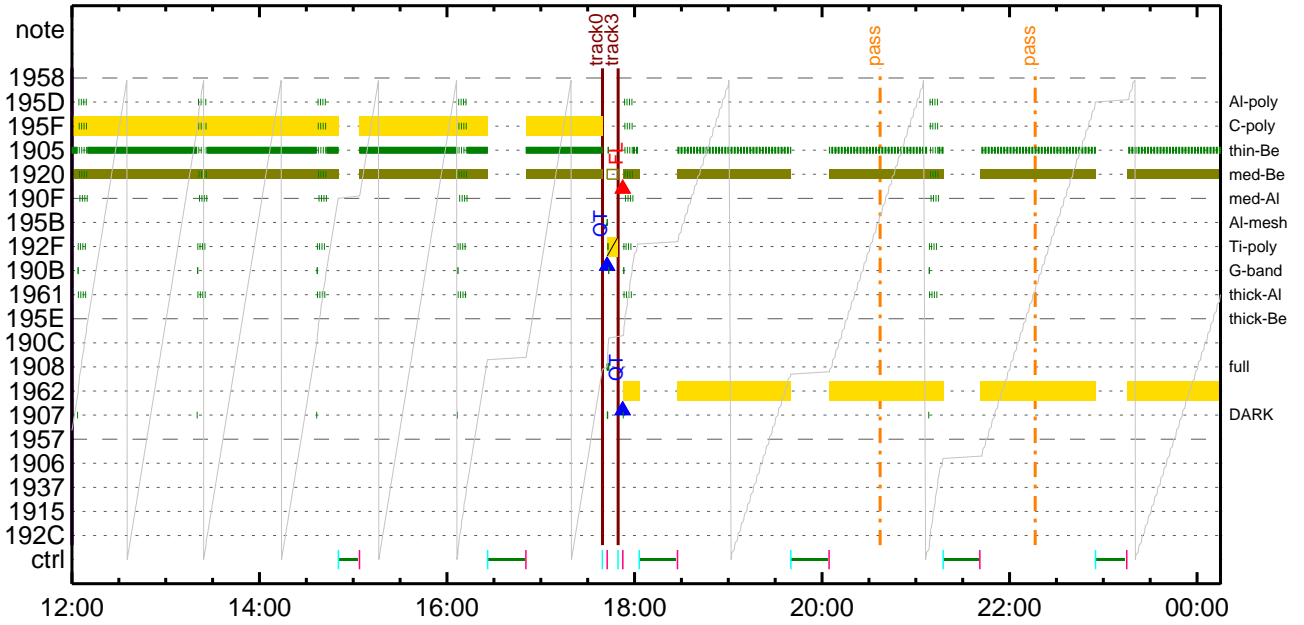
CMDI #0170 2013/01/10



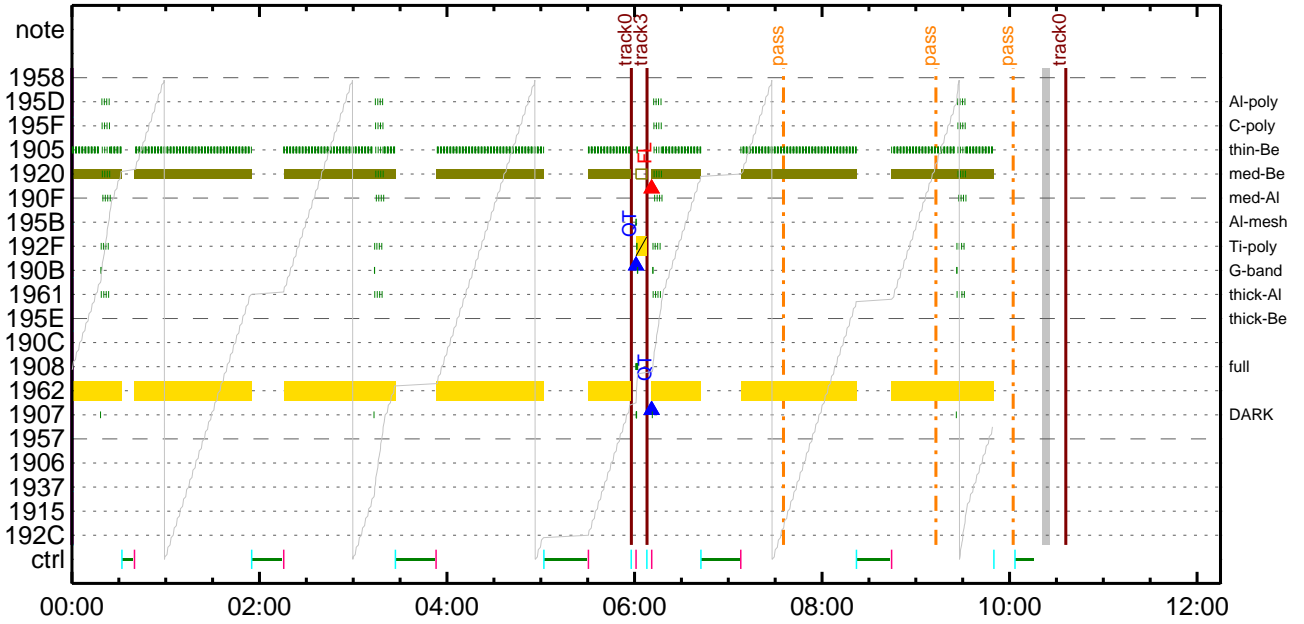
CMDI #0170 2013/01/11



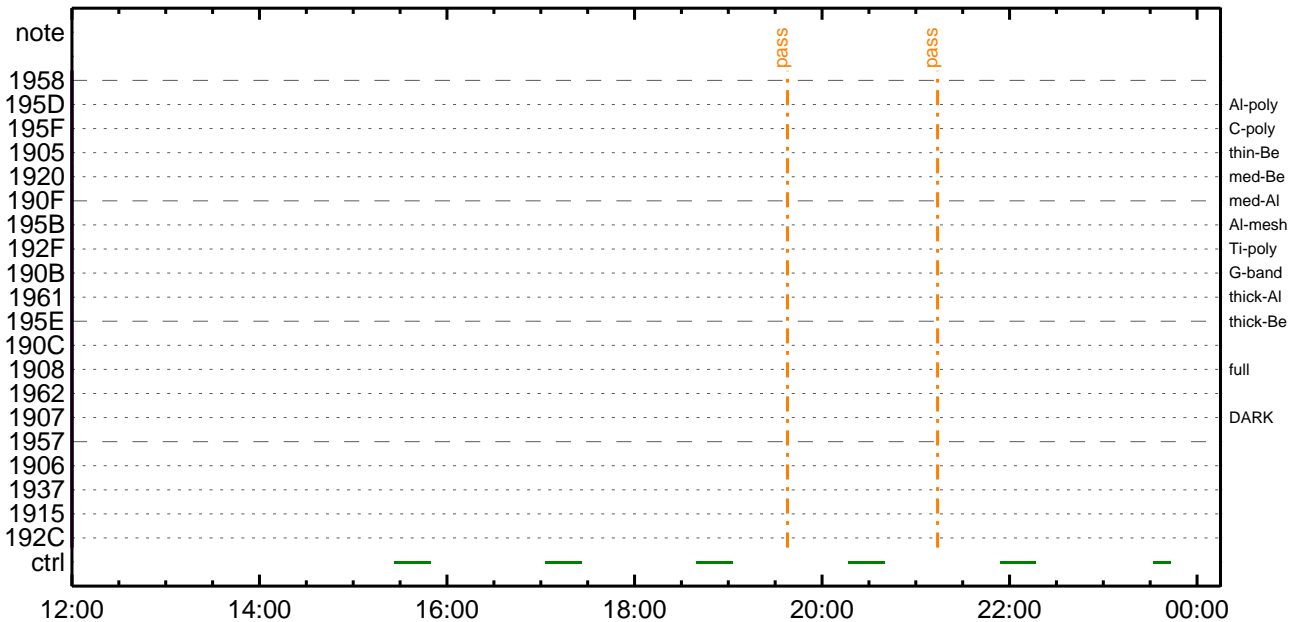
CMDI #0170 2013/01/11



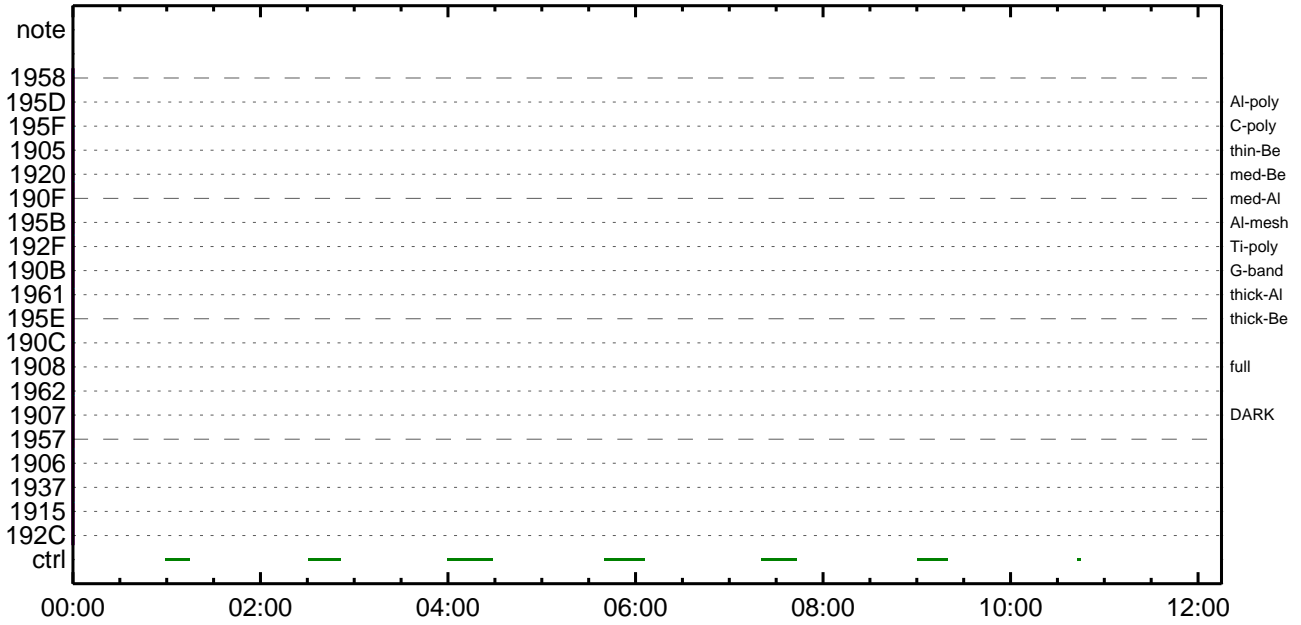
CMDI #0170 2013/01/12



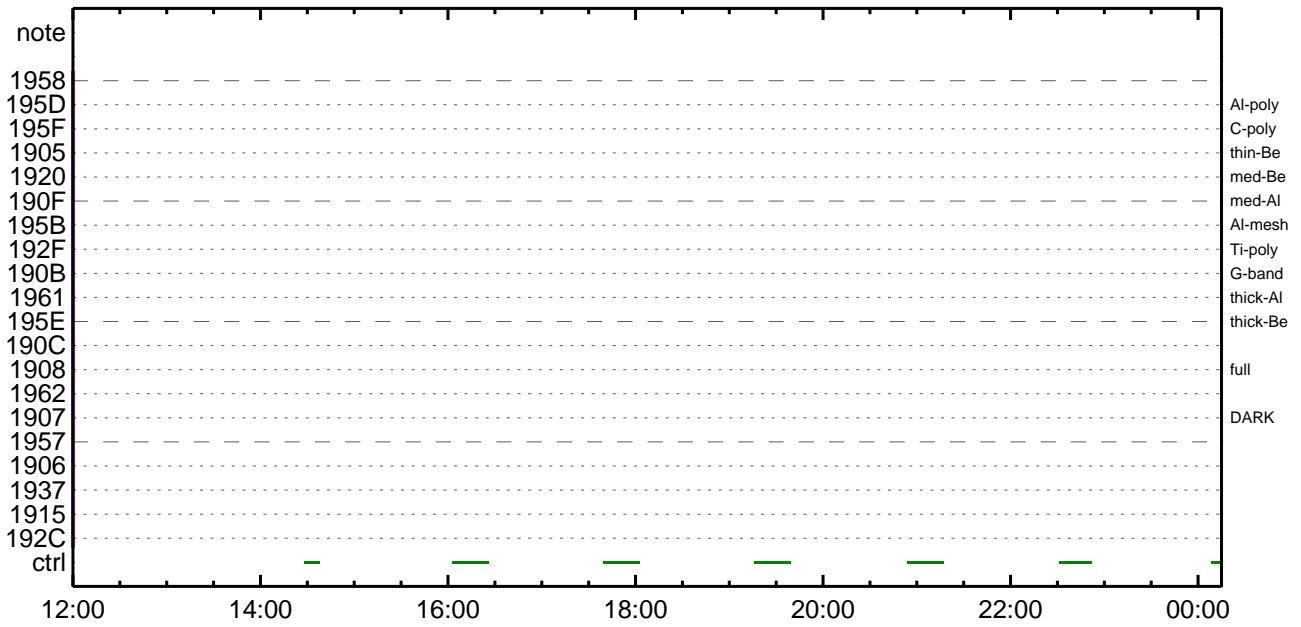
CMDI #0170 2013/01/12



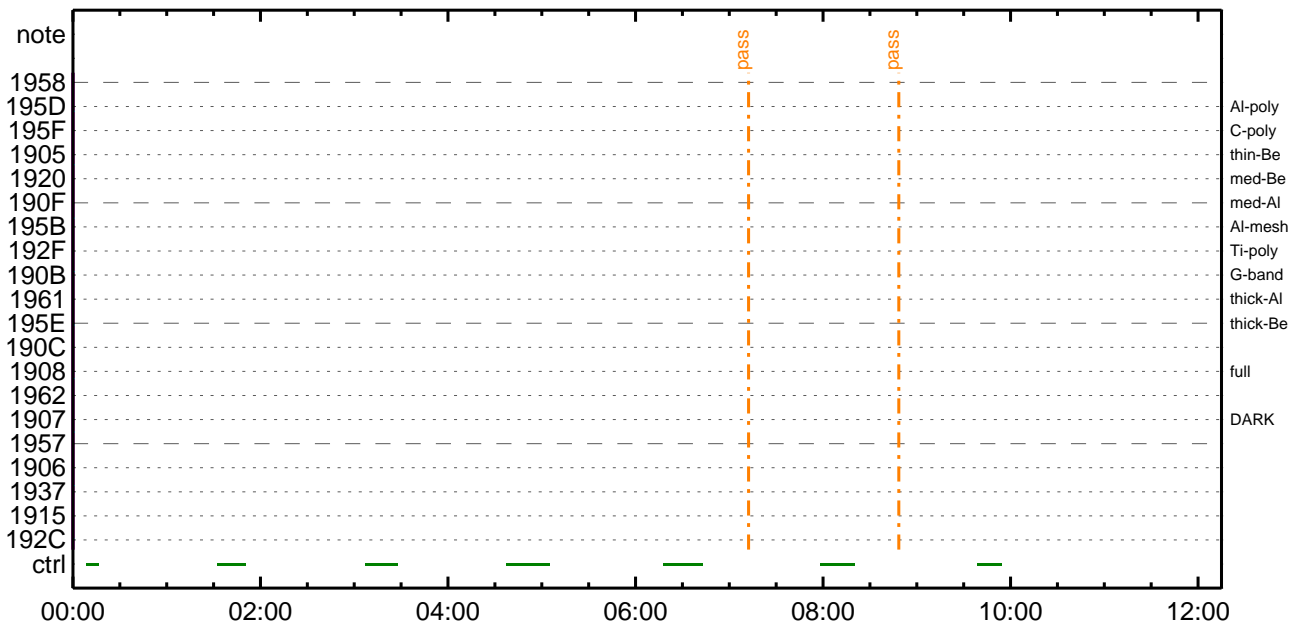
CMDI #0170 2013/01/13



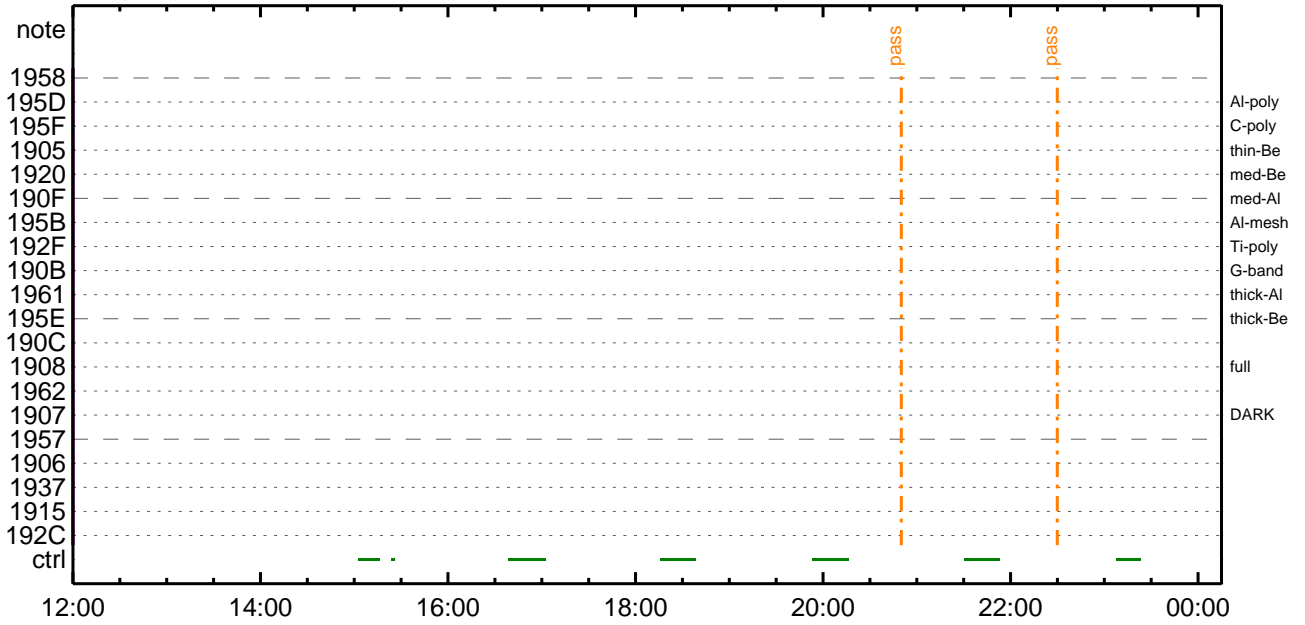
CMDI #0170 2013/01/13



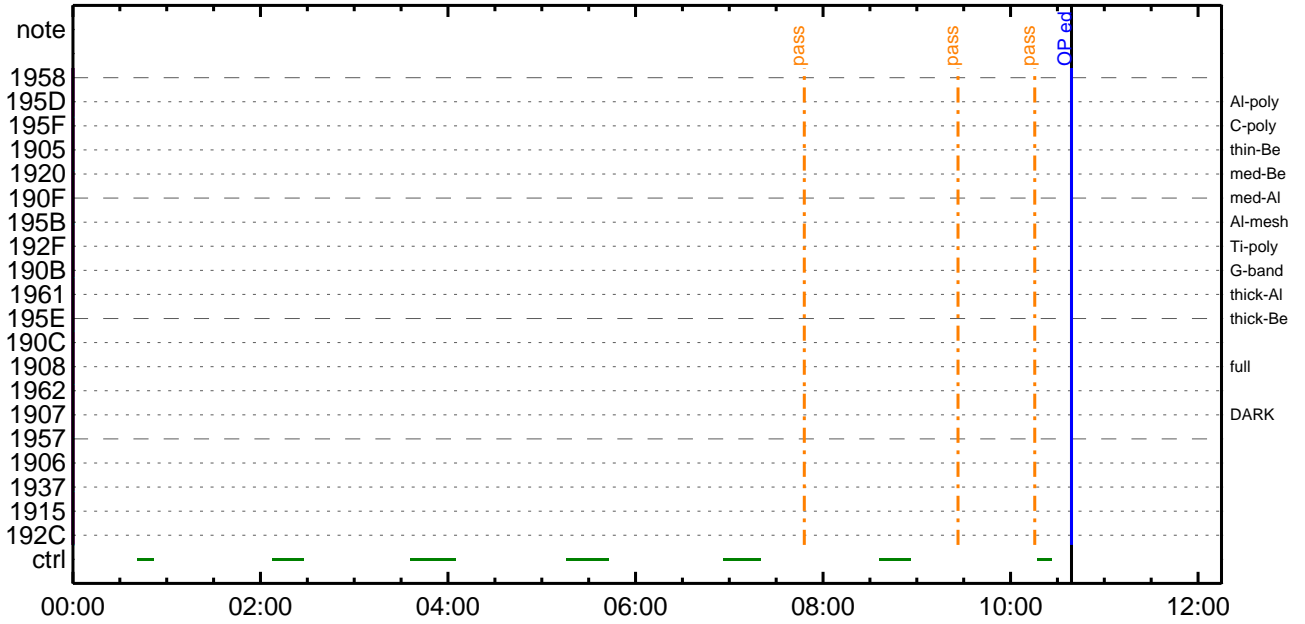
CMDI #0170 2013/01/14



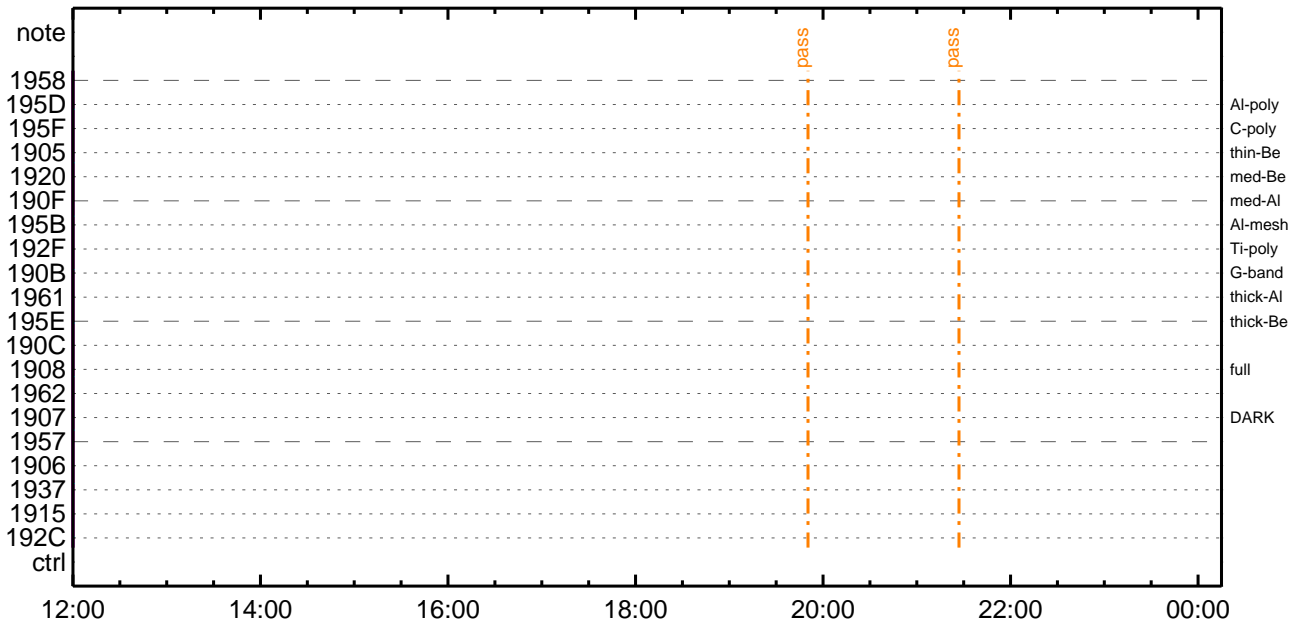
CMDI #0170 2013/01/14



CMDI #0170 2013/01/15



CMDI #0170 2013/01/15




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0096 C.
0097 C.
0098 C. *****
0099 C. OP/OGY1;4YE;|YAYOX
0100 C. *****
0101 C.
0102 . C. ;ãOP/OGY1;4YE;ã
0103 . S. OP op-381:OP
0104 ( )
0105 . S. OG og-381:OG
0106 ( )
0107 C.
0108 . C. ;ãNMOG&OPfî°èYAYOX;ã
0109 C. NMOG(0x200000-0x207FFF;§ 32 kbyte)
0110 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0111 BC (20 00 7f 01 02)
0112 C. çç[HK1_DMP_TOP_ADRS_1] EQ 40
0113 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0114 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0115 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0116 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0117 +. DC 01-22 DHU_MODE_CHNG
0118 BC (07 0b f8)
0119 C. çç[HK1_PKT_FORM_NO] EQ 7
0120 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0121 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0122 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0123 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0124 . C. YAYOXx½ªî»ò³îÇ§
0125 C. çç[HK1_DMP_CHK_FLG] EQ NON
0126 . C. RAM ID=NMOG²î½E¹ç•è²îOKò³îÇ§
0127 C.
0128 C. NMOG(0x208000-0x20FFFF;§ 32 kbyte)
0129 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0130 BC (20 80 7f 01 02)
0131 C. çç[HK1_DMP_TOP_ADRS_1] EQ 41
0132 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0133 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0134 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0135 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0136 +. DC 01-22 DHU_MODE_CHNG
0137 BC (07 0b f8)
0138 C. çç[HK1_PKT_FORM_NO] EQ 7
0139 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0140 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0141 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0142 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0143 . C. YAYOXx½ªî»ò³îÇ§
0144 C. çç[HK1_DMP_CHK_FLG] EQ NON
0145 . C. RAM ID=NMOG²î½E¹ç•è²îOKò³îÇ§
0146 C.
0147 C. NMOG(0x210000-0x2100FF;§ 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)
0148 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0149 BC (21 00 41 01 02)
0150 C. çç[HK1_DMP_TOP_ADRS_1] EQ 42
0151 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0152 C. çç[HK1_DMP_BLOCK_NUM] EQ 65
0153 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0154 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0155 +. DC 01-22 DHU_MODE_CHNG
0156 BC (07 0b f8)
0157 C. çç[HK1_PKT_FORM_NO] EQ 7
0158 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0159 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0160 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0161 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0162 . C. YAYOXx½ªî»ò³îÇ§
0163 C. çç[HK1_DMP_CHK_FLG] EQ NON
0164 . C. RAM ID=NMOG, RAM ID=OP²î½E¹ç•è²îOKò³îÇ§
0165 C.
0166 . C. ***** °E²¼òî½Ã´¶Á°òEÉ¬ò°Á÷¿® (¼åµ-YAYOXx½ê½çòðÁÓæòÇ¼ª°¬òè¼î¹çòÇòâ) *****
0167 C. DHUYâ;4YE;E½Y½, Yî;4YE;Eòðîã¹
0168 +. DC 01-22 DHU_MODE_CHNG
0169 BC (02 0a f8)
0170 C. çç[HK1_PKT_FORM_NO] EQ 2
0171 C. çç[HK1_PKT_GEN_TIME] EQ 0.5S
0172 C. çç[HK1_S_TLM_BIT_RATE] EQ 32K
0173 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0174 C.
0175 . C. *****
0176 C. TI-CMD SET (OPOG STOP/COPY/START)
0177 C. *****
0178 C.
0179 . C. NOTICE ;§ OPOG UPLOAD²-Á÷¿®NG²î½î¹ç;ç°E²¼òî½TI-CMDÁ÷¿®²î½Á¹Ô²•²E²²²³òE;f
0180 C. ²²²¿;çSET²E²DUMP²î½±°îYÑY¹²ç¹Ô²|²³²E;f
0181 C.
0182 . C. TIY³Y²Y³Y²E²òðÁDî¿(UT)
0183 +. TI 2013-01-10 10:45:00.0
0184 DC 01-B3 DHU_OP_STOP
0185 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0186 C.
0187 +. TI 2013-01-10 10:45:01.0
0188 DC 01-B4 DHU_OP_COPY
0189 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0190 C.
0191 +. TI 2013-01-10 10:45:01.0
0192 DC 01-B5 DHU_OPOG_COPY
0193 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP

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0194 C.
0195 +. TI 2013-01-10 10:49:59.5
0196 DC 01-B2 DHU_OP_START
0197 C.          çç[HK1_TI_CMD_NUM]                      EQ      1COUNTUP
0198 C.
0199 C. °Ê²¼ïãîÄë%îíññîîŷÄŷ§ŷÄŷ-¹àîŷ
0200 C.          çç[HK1_TI_CMD_ENA/DIS]                    EQ      ENA
0201 C.          çç[HK1_TI_CMD_NUM]                        EQ      4
0202 C.          çç[HK1_NEXT_EXEC_PIM]                     EQ      DHU
0203 C.          çç[HK1_NEXT_EXEC_DC]                       EQ      0xB3
0204 C.
0205 . C. *****
0206 C. TIîŷ°èŷÄŷÖŷ×
0207 C. *****
0208 C.
0209 C. TI_TBL(0x03AB00-0x03AEFF;§ 1024byte)
0210 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0211 BC      (03 ab 03 01 02)
0212 C.          çç[HK1_DMP_TOP_ADRS_1]                    EQ      07
0213 C.          çç[HK1_DMP_TOP_ADRS_0]                    EQ      2B
0214 C.          çç[HK1_DMP_BLOCK_NUM]                      EQ      3
0215 C.          çç[HK1_DMP_REPEAT_NUM]                     EQ      0
0216 C.          çç[HK1_DMA_DMP_PIM]                        EQ      DHU
0217 +. DC 01-22 DHU_MODE_CHNG
0218 BC      (07 0b f8)
0219 C.          çç[HK1_PKT_FORM_NO]                        EQ      7
0220 C.          çç[HK1_PKT_GEN_TIME]                       EQ      0.25 s
0221 C.          çç[HK1_S_TLM_BIT_RATE]                     EQ      32k
0222 C.          çç[HK1_X_TLM_BIT_RATE]                     EQ      4M
0223 C.          çç[HK1_DMP_CHK_FLG]                        EQ      EXEC
0224 C.
0225 . C. ŷÄŷÖŷ×½ªî»ò³îÇ§
0226 C.          çç[HK1_DMP_CHK_FLG]                        EQ      NON
0227 C.
0228 . C. RAM ID=TI_TBLñî½È¹ç•è²îOKò³îÇ§
0229 C.
0230 . C. DHUŷã;¼ŷÈ;È¼ŷ½.ŷî;¼ŷÈ;Èòðîãñ¹
0231 +. DC 01-22 DHU_MODE_CHNG
0232 BC      (02 0a f8)
0233 C.          çç[HK1_PKT_FORM_NO]                        EQ      2
0234 C.          çç[HK1_PKT_GEN_TIME]                       EQ      0.5S
0235 C.          çç[HK1_S_TLM_BIT_RATE]                     EQ      32K
0236 C.          çç[HK1_X_TLM_BIT_RATE]                     EQ      4M
0237 C.
0238 . C. Stop EIS observation and temporarily disable EIS mode changes
0239 C.
0240 C.
0241 C. ***** Start EIS operation (TI set) *****
0242 C. Execute, after the success of OP upload.
0243 C. Set EIS TI-commands
0244 +. TI 2013-01-10 10:49:30.0
0245 DC 07-FC EIS_MODE_MANU
0246 BC      (21 02)
0247 +. TI 2013-01-10 10:49:40.0
0248 DC 07-FC EIS_MODE_CHG_DIS
0249 BC      (22)
0250 . C.          [ ] [HK1_TI_CMD_NUM]                      EQ      2 COUNTUP
0251 C. ***** End EIS operation (TI set) *****
0252 C.
0253 C.
0254 C. *****
0255 C. SOT TI command set
0256 C. *****
0257 C. Execute, after the success of OP upload.
0258 +. TI 2013-01-10 10:49:16.0
0259 DC 07-F0 MDP_SOT_MODE_STBY
0260 BC      (41)
0261 . C. -----
0262 C.      HK1_TI_CMD_NUM          = 1 CNTUP [ ]
0263 C. -----
0264 C. ***** SOT END *****
0265 C.
0266 C. ***** XRT START *****
0267 C. Execute, after the success of OP upload.
0268 +. TI 2013-01-10 10:49:00.0
0269 DC 07-F0 MDP_XRT_MODE_STBY
0270 BC      (c3)
0271 . C.          [ ] [HK1_TI_CMD_NUM]                      EQ      1COUNTUP
0272 C.
0273 C. ***** XRT END *****
0274 C.
0275 . C. ***** MDP ´ûÃîãî»ö¼ŷñèÄðñ¹èDCBC•x²è *****
0276 C. (¼ã°îŷÖŷÄŷÈŷŷŷŷÄŷçŷèè¼ññ¼Ä»ŷñ¹è)
0277 . S. DC-BC dcbc-402:DCBC
0278 (MDP_known_event)
0279 C.
0280 C.
0281 . C. ***** ŷĐŷ¹•î Daily±çîññè´Øñ¹èDCBC•x²è *****
0282 . S. DC-BC dcbc-153:DCBC
0283 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0284 C.
0285 C.
0286 . C. ;ãLOSŷÄŷ§ŷÄŷ-¼Ä»ŷ;ã
0287 C.
0288 . C. ***** LOS *****
0289 C.
```

(a) Spacecraft Operation Procedure (real-commands)

```
main-382 2013-01-10 12:52:29 82 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. ;ãAOSYÁYŞYÄY-¼Ä»Û;ã
0005 C.
0006 C. YÀYB;¼Y³YFÝÓYÉÁ+¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCS : Reload orbital element (send every contact) *****
0010 C. Áí;È¿µÄµ°È»Í×ÁÇµÍYçYÄY×Yí;¼YÉ;ÈÈ%µ•íÉ;ÈÈ%°ÇÖµ•µ¿¼l¹çµÍ;çÄ®, ùµ¹µèµµµÇÁ+¿®µ•µÈµµµ³µÈ;f
0011 +. DC 02-8E AOCS_ORB_UPD
0012 C.
0013 C.
0014 . C. ***** AOCS Commands (Tracking Curve Upload) *****
0015 C. Upload the Orbit Element and the Target Attitude
0016 C. RAM-ID:TARGET_ATT
0017 . S. RAM ram-150:TARGET_ATT
0018 ( )
0019 C.
0020 C.
0021 C. Set the dump memory area of TARGET_ATT
0022 +. DC 02-48 AOCS_DUMP_SET
0023 BC (07 00 00 00 18 00)
0024 C.
0025 C. <A_STs1>[MEMORY OPERATE SATUS] ADRS = 070000 [ ]
0026 C.
0027 C.
0028 C. Change the TLMFormatNo for the AOCS Dump Format
0029 +. DC 01-22 DHU_MODE_CHNG
0030 BC (04 0b f8)
0031 C.
0032 C. Wait for AOCS DUMP to end
0033 C.
0034 . C. Check the dump memory
0035 C.
0036 C. Result = OK [ ]
0037 C.
0038 +. DC 01-22 DHU_MODE_CHNG
0039 BC (02 0a f8)
0040 C.
0041 C. <A_***>[TLM STS] FMT = 2 [ ]
0042 C.
0043 +. DC 02-8E AOCS_ORB_UPD
0044 . C.
0045 . C. Load OBSTBL, dump OBSTBL, enable EIS mode changes
0046 +. DC 07-FC EIS_MODE_MANU
0047 BC (21 02)
0048 . C. Verify EIS in MANUAL mode
0049 . C. Estimated OBSTBL upload time is 13s
0050 C. *****
0051 C. EIS START OBSTBL LOAD
0052 C. *****
0053 . S. RAM ram-820:EIS_OBSTBL
0054 ( )
0055 +. DC 07-FC EIS_DUMP_OBSTBL
0056 BC (07 07 07 00 00 70 00)
0057 C.
0058 C. Execute, after the success of OBSTBL upload.
0059 C. Set EIS TI-commands
0060 +. TI 2013-01-10 10:49:50.0
0061 DC 07-FC EIS_MODE_CHG_ENA
0062 BC (20)
0063 . C. [ ] [HK1_TI_CMD_NUM] EQ 1 COUNTUP
0064 C. *****
0065 C. EIS END OBSTBL LOAD
0066 C. *****
0067 C.
0068 . C. ***** MDP `ûÄîõî»ó%YµÈÄµ¹µèDCBC•x²è *****
0069 C. (%á°íYÓYÄYÈYÞYÉYáYçYèµÈ%¼µ¼Ä»Ûµ¹µè)
0070 . S. DC-BC dcbc-402:DCBC
0071 (MDP_known_event)
0072 C.
0073 C.
0074 . C. ***** YDÝ¹.Ï Daily±¿ÍÑµÈ´Øµ¹µèDCBC•x²è *****
0075 . S. DC-BC dcbc-153:DCBC
0076 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0077 C.
0078 C.
0079 . C. ;ãLOSÝÁYŞYÄY-¼Ä»Û;ã
0080 C.
0081 . C. ***** LOS *****
0082 C.
```



```

0096 C.
0097 C.
0098 C. *****
0099 C. SOT table upload
0100 C. *****
0101 . C. < Stop FG table >
0102 +. DC 07-F0 MDP_FG_CTRL_MANU
0103 BC (51)
0104 . C. -----
0105 C. MDP_FG_CTRL_MODE = MANU [ ]
0106 C. -----
0107 C.
0108 . C. <Upload FG Observation Table>
0109 . S. RAM ram-265:MDP_OBS_F
0110 ( )
0111 C.
0112 . C. < Dump RAMID=MDP_OBS_F >
0113 +. DC 07-F0 MDP_DUMP_FGTBL
0114 BC (82 07 00 00 00 38 b8)
0115 C. -----
0116 C. MDP_OBS_F verify = OK/NG [ ]
0117 C. -----
0118 C.
0119 . C. < Stop SP table >
0120 +. DC 07-F0 MDP_SP_CTRL_MANU
0121 BC (61)
0122 C. -----
0123 C. MDP_SP_CTRL_MODE = MANU [ ]
0124 C. -----
0125 C.
0126 . C. <Upload SP Observation Table>
0127 . S. RAM ram-286:MDP_OBS_S
0128 ( )
0129 C.
0130 . C. < Dump RAMID=MDP_OBS_S >
0131 +. DC 07-F0 MDP_DUMP_SPTBL
0132 BC (83 07 00 00 00 38 b8)
0133 C. -----
0134 C. MDP_OBS_S verify = OK/NG [ ]
0135 C. -----
0136 C.
0137 C. *****
0138 C. SOT TI command set
0139 C. *****
0140 C. Execute, after the success of TBL upload.
0141 +. TI 2013-01-10 10:49:18.0
0142 DC 07-F0 MDP_SOT_MODE_OBSV
0143 BC (40)
0144 . C. -----
0145 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0146 C. -----
0147 C.
0148 C.
0149 C. ***** XRT START *****
0150 C.
0151 +. DC 07-F0 MDP_XRT_CTRL_MANU
0152 BC (c1)
0153 + DC 07-F0 MDP_XRT_MODE_STBY
0154 BC (c3)
0155 . C. ----- Success Verify ? OK / NG____
0156 C.
0157 C. XRT Obs. Table Upload
0158 . S. RAM ram-291:MDP_OBS_X
0159 ( )
0160 C.
0161 +. DC 07-F0 MDP_DUMP_XRTTBL
0162 BC (84 07 00 00 00 3a d4)
0163 . C. ----- Comparison Check ? OK / ERR ____
0164 C.
0165 C.
0166 +. DC 07-F0 MDP_XRT_ROI_SET
0167 BC (cd 01 b1 b1 04 04)
0168 + DC 07-F0 MDP_XRT_ROI_SET
0169 BC (cd 02 b1 b1 08 08)
0170 + DC 07-F0 MDP_XRT_ROI_SET
0171 BC (cd 03 b1 b1 08 08)
0172 + DC 07-F0 MDP_XRT_ROI_SET
0173 BC (cd 04 b1 b1 06 06)
0174 + DC 07-F0 MDP_XRT_ROI_SET
0175 BC (cd 05 85 83 06 06)
0176 + DC 07-F0 MDP_XRT_ROI_SET
0177 BC (cd 06 85 83 06 06)
0178 + DC 07-F0 MDP_XRT_ROI_SET
0179 BC (cd 07 85 83 08 08)
0180 + DC 07-F0 MDP_XRT_ROI_SET
0181 BC (cd 08 80 80 20 20)
0182 + DC 07-F0 MDP_XRT_ROI_SET
0183 BC (cd 09 80 80 20 08)
0184 + DC 07-F0 MDP_XRT_ROI_SET
0185 BC (cd 0a 80 80 08 20)
0186 + DC 07-F0 MDP_XRT_ROI_SET
0187 BC (cd 0f 80 80 06 06)
0188 + DC 07-F0 MDP_XRT_ROI_SET
0189 BC (cd 10 80 80 08 08)
0190 + DC 07-F0 MDP_XRT_FLD_ENA
0191 BC (d8)
0192 + DC 07-F0 MDP_XRT_FLRCTRL_ENA
0193 BC (c8)

```

```
0194 + DC 07-F0 MDP_XRT_AEC_RESET
0195 BC (d0)
0196 + DC 07-F0 MDP_XRT_ARS_DIS
0197 BC (d5)
0198 + DC 07-F0 MDP_XRT_FLD_RESET
0199 BC (da)
0200 + DC 07-F0 MDP_XRT_QT_PROG_SET
0201 BC (c4 12)
0202 +. DC 07-F0 MDP_XRT_FL_PROG_SET
0203 BC (c5 10)
0204 . C. ----- Success Verify ? OK / NG ____
0205 C.
0206 C.
0207 . C. All OK? Yes--> Please Proceed. / No --> Stop here.
0208 C.
0209 +. DC 07-F0 MDP_XRT_MODE_OBSV
0210 BC (c2)
0211 +. TI 2013-01-10 10:49:02.0
0212 DC 07-F0 MDP_XRT_MODE_OBSV
0213 BC (c2)
0214 . C. ----- Success Verify ? OK / NG ____
0215 C.
0216 C. ***** XRT END *****
0217 C.
0218 . C. ***** MDP `úÃîñî»ö%ÝñÊÃð¹ñèDCBC•x²è *****
0219 C. (%á°îÝÓÝÃÝÈÝÞÝËÝáÝçÝèñÊ¼ññ¼Ã»Ûñ¹ñè)
0220 . S. DC-BC dcbc-402:DCBC
0221 (MDP_known_event)
0222 C.
0223 C.
0224 . C. ***** ÝDÝ¹•Ï Daily±¿îÑñÊ´Øñ¹ñèDCBC•x²è *****
0225 . S. DC-BC dcbc-153:DCBC
0226 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0227 C.
0228 C.
0229 . C. ¡ãLOSÝÁÝ$ÝÃÝ-¼Ã»Ûñ¹ñè
0230 C.
0231 . C. ***** LOS *****
0232 C.
```

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*** OP Sequence for XRT ***

2013/01/10	10:59:54.0	XRT_CTRL_MANU_447_OG [0x1bf]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	11:00:00.0	AOCS_Ore-point_Start_1_OG [0x097]							
		AOCU_NM	5	02-76	00 b1 82 01 58				
2013/01/10	11:02:26.0	XRT_FOCUS_POSITION_420_OG [0x1a4]							
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00				
2013/01/10	11:02:46.0	XRT_FLD_ENA_418_OG [0x1a2]							
		MDP_XRT_FLD_ENA	1	07-F0	d8				
2013/01/10	11:02:48.0	XRT_FLRCTRL_ENA_401_OG [0x191]							
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8				
2013/01/10	11:02:50.0	XRT_AEC_RESET_423_OG [0x1a7]							
		MDP_XRT_AEC_RESET	1	07-F0	d0				
2013/01/10	11:02:52.0	XRT_ARS_DIS_412_OG [0x19c]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/10	11:02:54.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/10	11:02:56.0	XRT_QT_PROG_SET_435_OG [0x1b3]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0f				
2013/01/10	11:02:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]							
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 10				
2013/01/10	11:03:00.0	XRT_CTRL_AUTO_408_OG [0x198]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/10	14:16:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	14:16:02.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/10	14:16:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/10	14:19:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/10	14:24:00.0	XRT_Custom_434_OG [0x1b2]							
2013/01/10	14:25:00.0	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/10	15:49:30.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	15:49:32.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/10	15:49:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/10	15:52:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/10	16:13:00.0	XRT_Custom_434_OG [0x1b2]							
2013/01/10	16:14:00.0	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/10	16:59:54.0	XRT_CTRL_MANU_402_OG [0x192]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	16:59:56.0	XRT_FOCUS_POSITION_420_OG [0x1a4]							
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00				
2013/01/10	17:00:00.0	AOCS_Ore-point_Start_2_OG [0x098]							
		AOCU_NM	5	02-76	03 00 00 00 00				
2013/01/10	17:00:16.0	XRT_FLD_ENA_428_OG [0x1ac]							
		MDP_XRT_FLD_ENA	1	07-F0	d8				
2013/01/10	17:00:18.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]							
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8				
2013/01/10	17:00:20.0	XRT_AEC_RESET_423_OG [0x1a7]							
		MDP_XRT_AEC_RESET	1	07-F0	d0				
2013/01/10	17:00:22.0	XRT_ARS_DIS_437_OG [0x1b5]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/10	17:02:54.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/10	17:02:56.0	XRT_QT_PROG_SET_422_OG [0x1a6]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 12				
2013/01/10	17:02:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]							
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 10				
2013/01/10	17:03:00.0	XRT_CTRL_AUTO_408_OG [0x198]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/10	17:26:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	17:26:02.0	XRT_FLD_RESET_424_OG [0x1a8]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2013/01/10	17:26:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2013/01/10	17:29:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2013/01/10	17:49:30.0	XRT_Custom_434_OG [0x1b2]							
2013/01/10	17:50:30.0	XRT_CTRL_AUTO_413_OG [0x19d]							
		MDP_XRT_CTRL_AUTO	1	07-F0	c0				
2013/01/10	18:05:54.0	XRT_CTRL_MANU_402_OG [0x192]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2013/01/10	18:05:56.0	XRT_FOCUS_POSITION_403_OG [0x193]							
		XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00				
2013/01/10	18:06:00.0	AOCS_Ore-point_Start_3_OG [0x099]							
		AOCU_NM	5	02-76	00 00 00 00 00				
2013/01/10	18:06:16.0	XRT_FLD_DIS_404_OG [0x194]							
		MDP_XRT_FLD_DIS	1	07-F0	d9				
2013/01/10	18:06:18.0	XRT_FLRCTRL_DIS_405_OG [0x195]							
		MDP_XRT_FLRCTRL_DIS	1	07-F0	c9				
2013/01/10	18:06:20.0	XRT_ARS_DIS_406_OG [0x196]							
		MDP_XRT_ARS_DIS	1	07-F0	d5				
2013/01/10	18:08:58.0	XRT_QT_PROG_SET_419_OG [0x1a3]							
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d				

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2013/01/10	18:09:00.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/10	18:15:54.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/10	18:15:56.0	XRT_FOCUS_POSITION_420_OG [0x1a4]			
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2013/01/10	18:16:00.0	AOCS_Ore-point_Start_2_OG [0x098]			
		AOCU_NM	5	02-76	03 00 00 00 00
2013/01/10	18:16:16.0	XRT_FLD_ENA_428_OG [0x1ac]			
		MDP_XRT_FLD_ENA	1	07-F0	d8
2013/01/10	18:16:18.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]			
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2013/01/10	18:16:20.0	XRT_AEC_RESET_423_OG [0x1a7]			
		MDP_XRT_AEC_RESET	1	07-F0	d0
2013/01/10	18:16:22.0	XRT_ARS_DIS_437_OG [0x1b5]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/10	18:18:54.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/10	18:18:56.0	XRT_QT_PROG_SET_422_OG [0x1a6]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 12
2013/01/10	18:18:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]			
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 10
2013/01/10	18:19:00.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/10	19:03:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/10	19:03:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/10	19:03:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/10	19:06:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/10	19:26:30.0	XRT_Custom_434_OG [0x1b2]			
2013/01/10	19:27:30.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/10	20:40:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/10	20:40:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/10	20:40:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/10	20:43:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/10	21:04:00.5	XRT_Custom_434_OG [0x1b2]			
2013/01/10	21:05:00.5	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/10	22:18:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/10	22:18:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/10	22:18:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/10	22:21:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/10	22:39:30.0	XRT_Custom_434_OG [0x1b2]			
2013/01/10	22:40:30.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/10	23:55:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/10	23:55:32.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/10	23:55:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/10	23:58:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	00:04:00.5	XRT_Custom_434_OG [0x1b2]			
2013/01/11	00:05:00.5	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	01:20:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	01:20:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	01:20:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	01:23:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	01:38:00.0	XRT_Custom_434_OG [0x1b2]			
2013/01/11	01:39:00.0	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	02:54:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	02:54:02.0	XRT_FLD_RESET_424_OG [0x1a8]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	02:54:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	02:57:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	03:15:00.5	XRT_Custom_434_OG [0x1b2]			
2013/01/11	03:16:00.5	XRT_CTRL_AUTO_413_OG [0x19d]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	04:24:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	04:24:02.0	XRT_FLD_RESET_424_OG [0x1a8]			

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2013/01/11	04:24:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	04:27:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	04:52:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	04:53:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	05:36:24.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	05:36:26.0	XRT_FOCUS_POSITION_403_OG [0x193]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00
2013/01/11	05:36:30.0	AOCS_Ore-point_Start_3_OG [0x099]	AOCU_NM	5	02-76	00 00 00 00 00
2013/01/11	05:36:46.0	XRT_FLD_DIS_404_OG [0x194]	MDP_XRT_FLD_DIS	1	07-F0	d9
2013/01/11	05:36:48.0	XRT_FLRCTRL_DIS_405_OG [0x195]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9
2013/01/11	05:36:50.0	XRT_ARS_DIS_406_OG [0x196]	MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/11	05:39:28.0	XRT_QT_PROG_SET_419_OG [0x1a3]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d
2013/01/11	05:39:30.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	05:46:24.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	05:46:26.0	XRT_FOCUS_POSITION_420_OG [0x1a4]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2013/01/11	05:46:30.0	AOCS_Ore-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	03 00 00 00 00
2013/01/11	05:46:46.0	XRT_FLD_ENA_428_OG [0x1ac]	MDP_XRT_FLD_ENA	1	07-F0	d8
2013/01/11	05:46:48.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2013/01/11	05:46:50.0	XRT_AEC_RESET_423_OG [0x1a7]	MDP_XRT_AEC_RESET	1	07-F0	d0
2013/01/11	05:46:52.0	XRT_ARS_DIS_437_OG [0x1b5]	MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/11	05:49:24.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	05:49:26.0	XRT_QT_PROG_SET_422_OG [0x1a6]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 12
2013/01/11	05:49:28.0	XRT_FL_PROG_SET_444_OG [0x1bc]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 10
2013/01/11	05:49:30.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	06:04:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	06:04:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	06:04:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	06:07:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	06:30:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	06:31:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	07:45:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	07:45:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	07:45:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	07:48:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	08:07:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	08:08:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	09:24:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	09:24:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	09:24:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	09:27:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	09:42:00.5	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	09:43:00.5	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	14:50:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	14:50:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	14:50:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	14:53:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	15:03:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	15:04:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	16:26:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	16:26:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_CTRL_MANU	1	07-F0	c1

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2013/01/11	16:26:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	16:29:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	16:49:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	16:50:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	17:39:24.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	17:39:26.0	XRT_FOCUS_POSITION_403_OG [0x193]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00
2013/01/11	17:39:30.0	AOCS_OrE-point_Start_3_OG [0x099]	AOCU_NM	5	02-76	00 00 00 00 00
2013/01/11	17:39:46.0	XRT_FLD_DIS_404_OG [0x194]	MDP_XRT_FLD_DIS	1	07-F0	d9
2013/01/11	17:39:48.0	XRT_FLRCTRL_DIS_405_OG [0x195]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9
2013/01/11	17:39:50.0	XRT_ARS_DIS_406_OG [0x196]	MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/11	17:42:28.0	XRT_QT_PROG_SET_419_OG [0x1a3]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d
2013/01/11	17:42:30.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	17:49:24.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	17:49:26.0	XRT_FOCUS_POSITION_420_OG [0x1a4]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2013/01/11	17:49:30.0	AOCS_OrE-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	03 00 00 00 00
2013/01/11	17:49:46.0	XRT_FLD_ENA_428_OG [0x1ac]	MDP_XRT_FLD_ENA	1	07-F0	d8
2013/01/11	17:49:48.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2013/01/11	17:49:50.0	XRT_AEC_RESET_423_OG [0x1a7]	MDP_XRT_AEC_RESET	1	07-F0	d0
2013/01/11	17:49:52.0	XRT_ARS_DIS_437_OG [0x1b5]	MDP_XRT_ARS_DIS	1	07-F0	d5
2013/01/11	17:52:24.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	17:52:26.0	XRT_QT_PROG_SET_430_OG [0x1ae]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 07
2013/01/11	17:52:28.0	XRT_FL_PROG_SET_444_OG [0x1bc]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 10
2013/01/11	17:52:30.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	18:03:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	18:03:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	18:03:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	18:06:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	18:26:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	18:27:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	19:40:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	19:40:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	19:40:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	19:43:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	20:03:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	20:04:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	21:17:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	21:17:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	21:17:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	21:20:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	21:40:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	21:41:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/11	22:55:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/11	22:55:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/11	22:55:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/11	22:58:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	23:14:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/11	23:15:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/12	00:32:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/12	00:32:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_CTRL_MANU	1	07-F0	c1

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2013/01/12	00:32:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	00:35:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/12	00:39:00.5	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/12	00:40:00.5	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	01:55:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	01:55:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	01:55:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/12	01:58:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/12	02:14:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	02:15:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	03:27:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	03:27:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	03:27:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/12	03:30:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/12	03:52:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	03:53:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	05:02:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	05:02:02.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	05:02:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/12	05:05:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/12	05:29:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	05:30:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	05:57:54.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	05:57:56.0	XRT_FOCUS_POSITION_403_OG [0x193]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00		
2013/01/12	05:58:00.0	AOCS_OrE-point_Start_3_OG [0x099]	AOCU_NM	5	02-76	00 00 00 00 00		
2013/01/12	05:58:16.0	XRT_FLD_DIS_404_OG [0x194]	MDP_XRT_FLD_DIS	1	07-F0	d9		
2013/01/12	05:58:18.0	XRT_FLRCTRL_DIS_405_OG [0x195]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9		
2013/01/12	05:58:20.0	XRT_ARS_DIS_406_OG [0x196]	MDP_XRT_ARS_DIS	1	07-F0	d5		
2013/01/12	06:00:58.0	XRT_QT_PROG_SET_419_OG [0x1a3]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d		
2013/01/12	06:01:00.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	06:07:54.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	06:07:56.0	XRT_FOCUS_POSITION_420_OG [0x1a4]	XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00		
2013/01/12	06:08:00.0	AOCS_OrE-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	03 00 00 00 00		
2013/01/12	06:08:16.0	XRT_FLD_ENA_428_OG [0x1ac]	MDP_XRT_FLD_ENA	1	07-F0	d8		
2013/01/12	06:08:18.0	XRT_FLRCTRL_ENA_429_OG [0x1ad]	MDP_XRT_FLRCTRL_ENA	1	07-F0	c8		
2013/01/12	06:08:20.0	XRT_AEC_RESET_423_OG [0x1a7]	MDP_XRT_AEC_RESET	1	07-F0	d0		
2013/01/12	06:08:22.0	XRT_ARS_DIS_437_OG [0x1b5]	MDP_XRT_ARS_DIS	1	07-F0	d5		
2013/01/12	06:10:54.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	06:10:56.0	XRT_QT_PROG_SET_430_OG [0x1ae]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 07		
2013/01/12	06:10:58.0	XRT_FL_PROG_SET_444_OG [0x1bc]	MDP_XRT_FL_PROG_SET	2	07-F0	c5 10		
2013/01/12	06:11:00.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	06:42:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	06:42:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da		
2013/01/12	06:42:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2013/01/12	06:45:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2013/01/12	07:07:00.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2013/01/12	07:08:00.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	08:22:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1		
2013/01/12	08:22:02.0	XRT_FLD_RESET_424_OG [0x1a8]						

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2013/01/12	08:22:04.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/12	08:25:14.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/12	08:43:30.0	XRT_Custom_434_OG [0x1b2]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/12	08:44:30.0	XRT_CTRL_AUTO_413_OG [0x19d]	MDP_XRT_CTRL_AUTO	1	07-F0	c0
2013/01/12	09:50:00.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/12	10:03:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1
2013/01/12	10:03:32.0	XRT_FLD_RESET_424_OG [0x1a8]	MDP_XRT_FLD_RESET	1	07-F0	da
2013/01/12	10:03:34.0	XRT_PREFLR_STRT_432_OG [0x1b0]	MDP_XRT_PREFLR_STRT	1	07-F0	e8
2013/01/12	10:06:44.0	XRT_PREFLR_STOP_433_OG [0x1b1]	MDP_XRT_PREFLR_STOP	1	07-F0	e9
2013/01/12	10:36:00.0	AOCS_ORe-point_Start_3_OG [0x099]	AOCU_NM	5	02-76	00 00 00 00 00