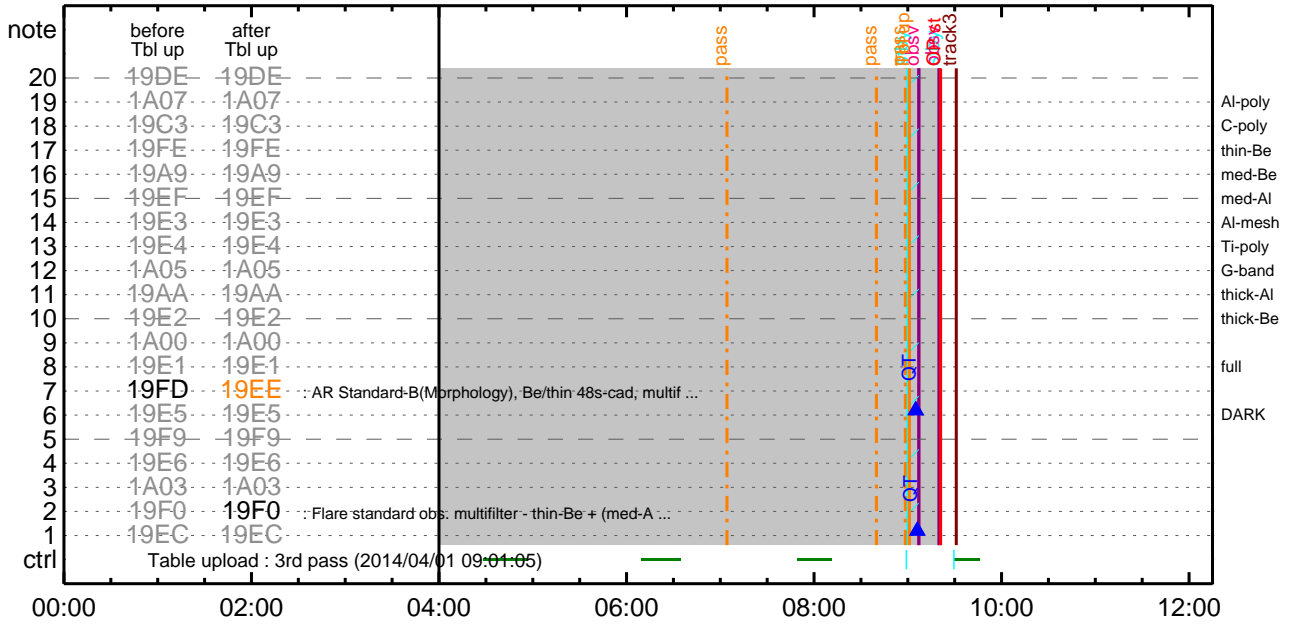


XRT Timeline to be uploaded on 2014/04/01

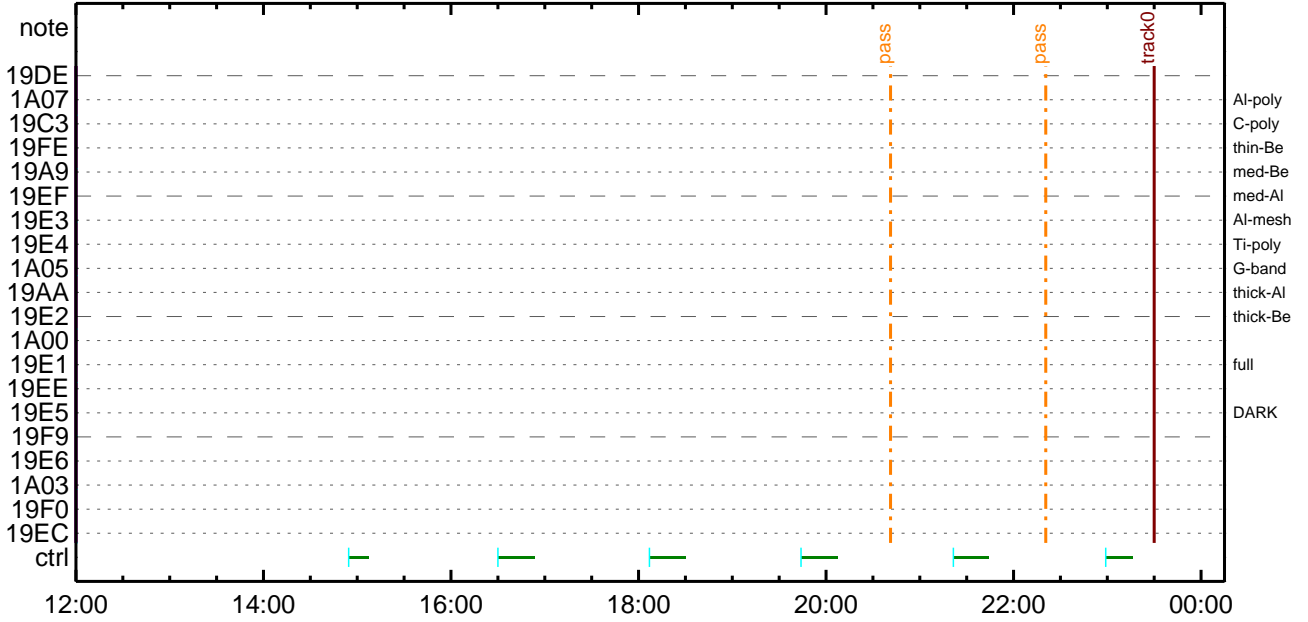
Period: 2014/04/01 09:21:00 - 2014/04/05 10:41:00

* * * * *	Normal mode	* * * * *
	NOT USED	
* * * * *	Flare mode	* * * * *
	NOT USED	
* * * * *	Active Region Search	* * * * *
	NOT USED	
* * * * *	Flare Detection	* * * * *
	NOT USED	

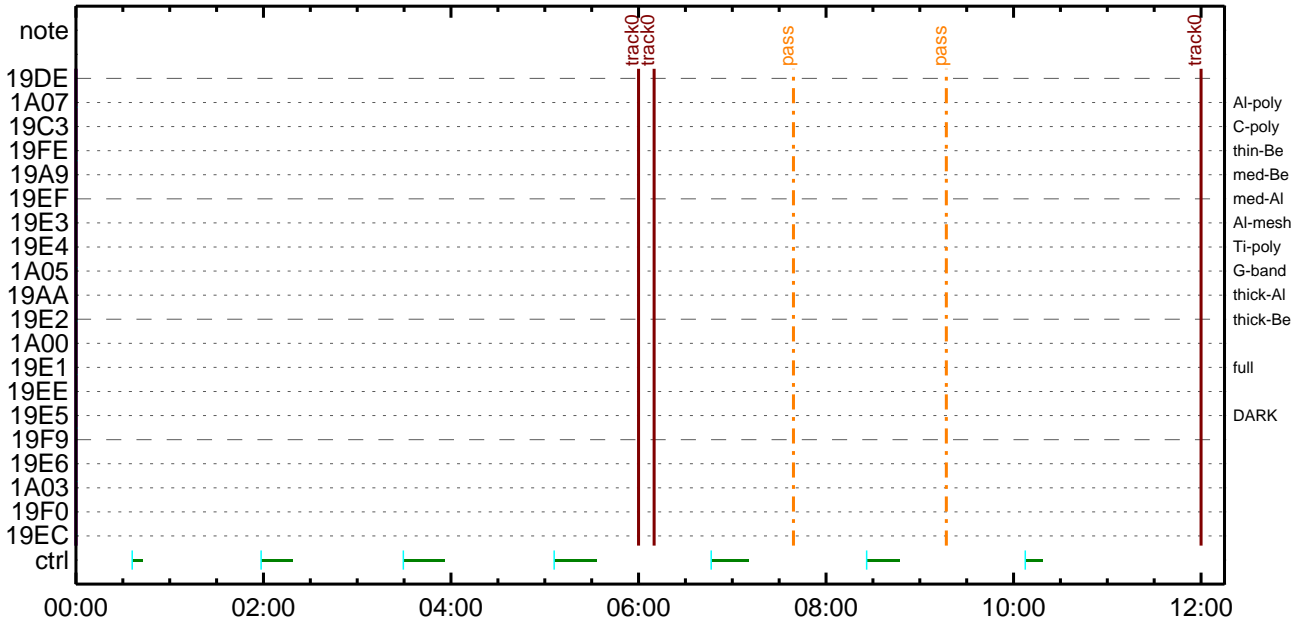
CMDI #0189 2014/04/01



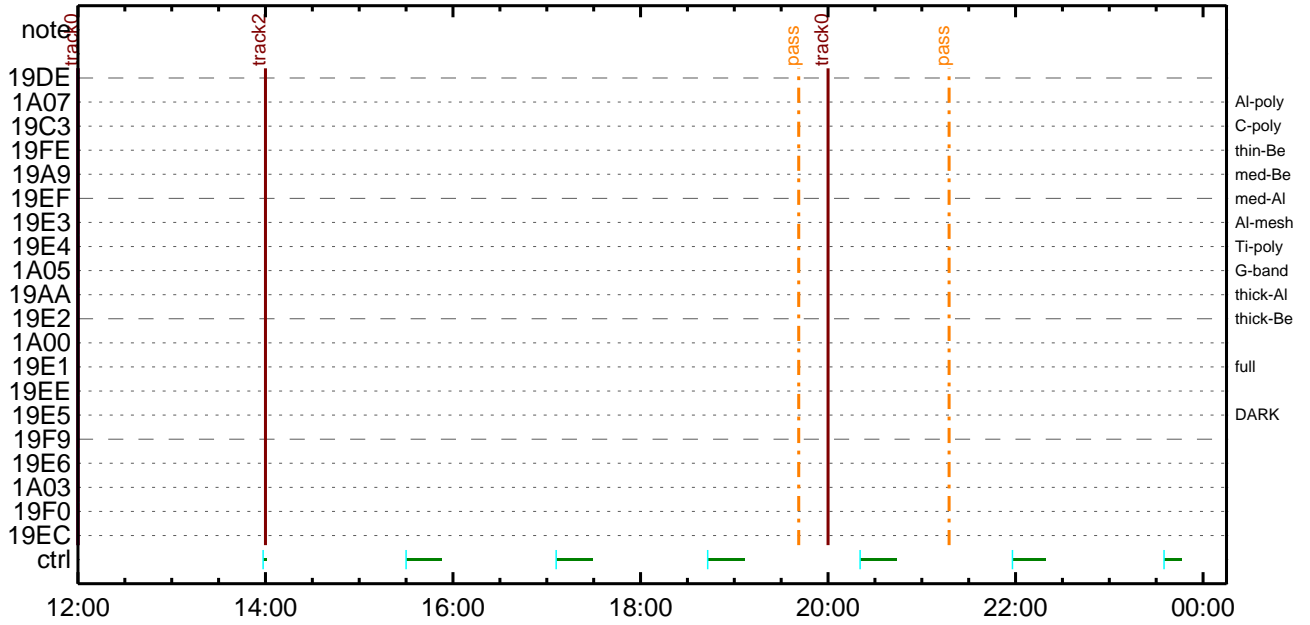
CMDI #0189 2014/04/01



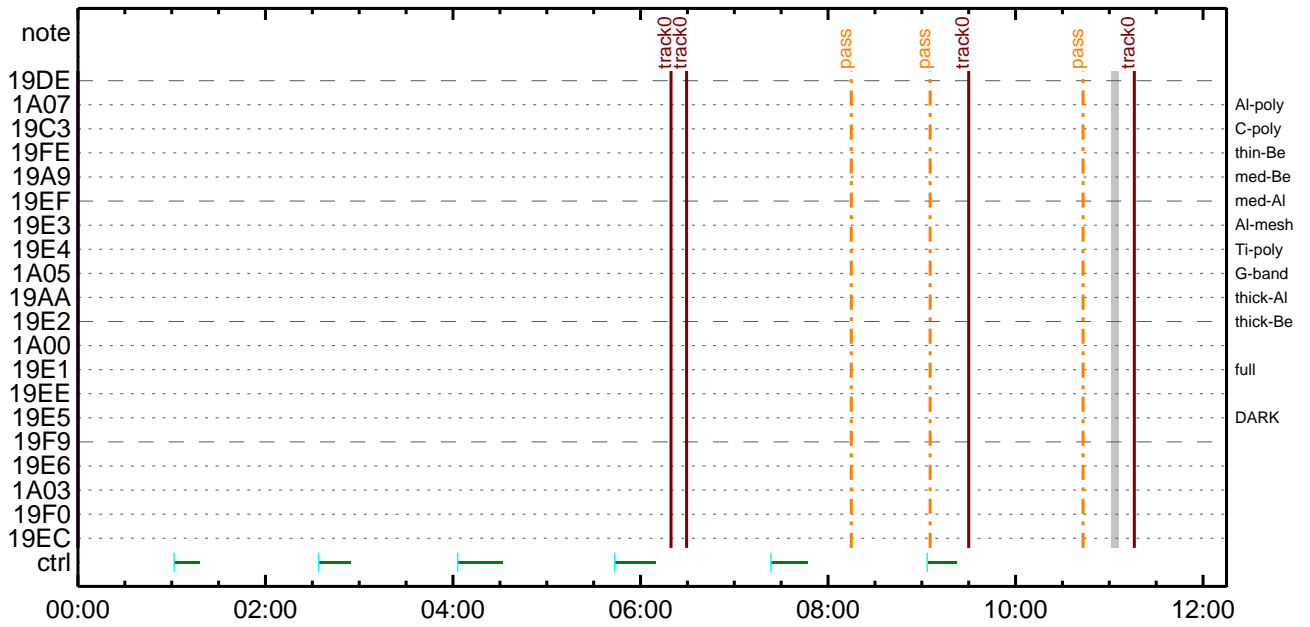
CMDI #0189 2014/04/02



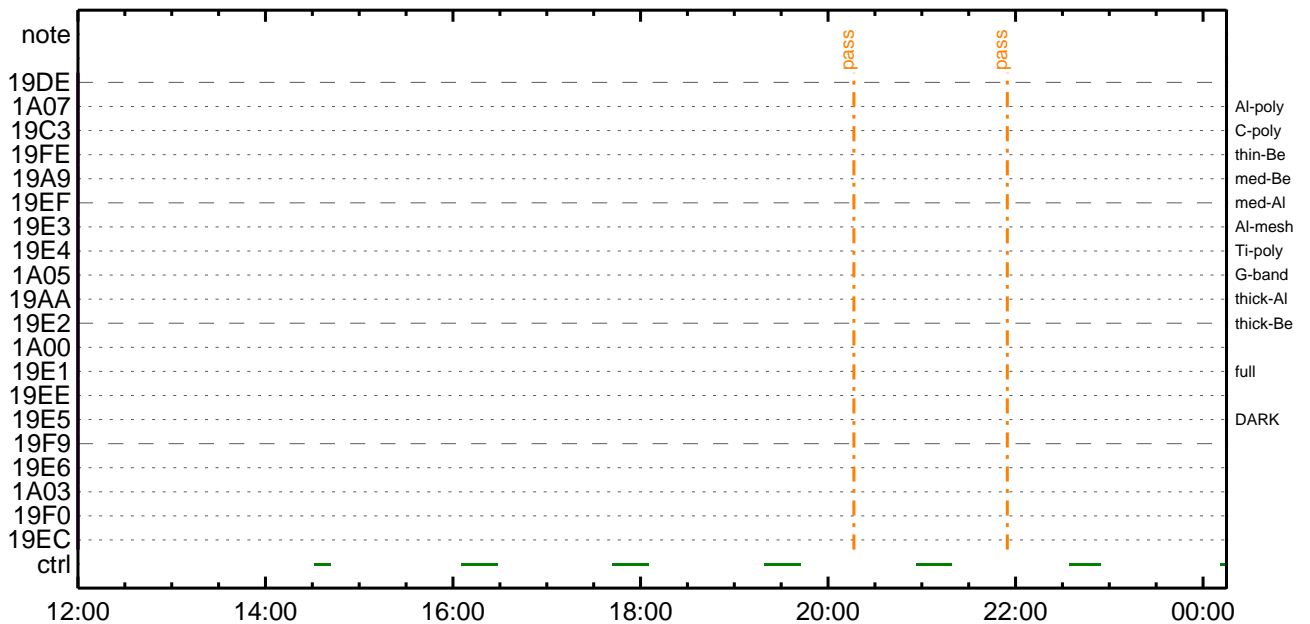
CMDI #0189 2014/04/02



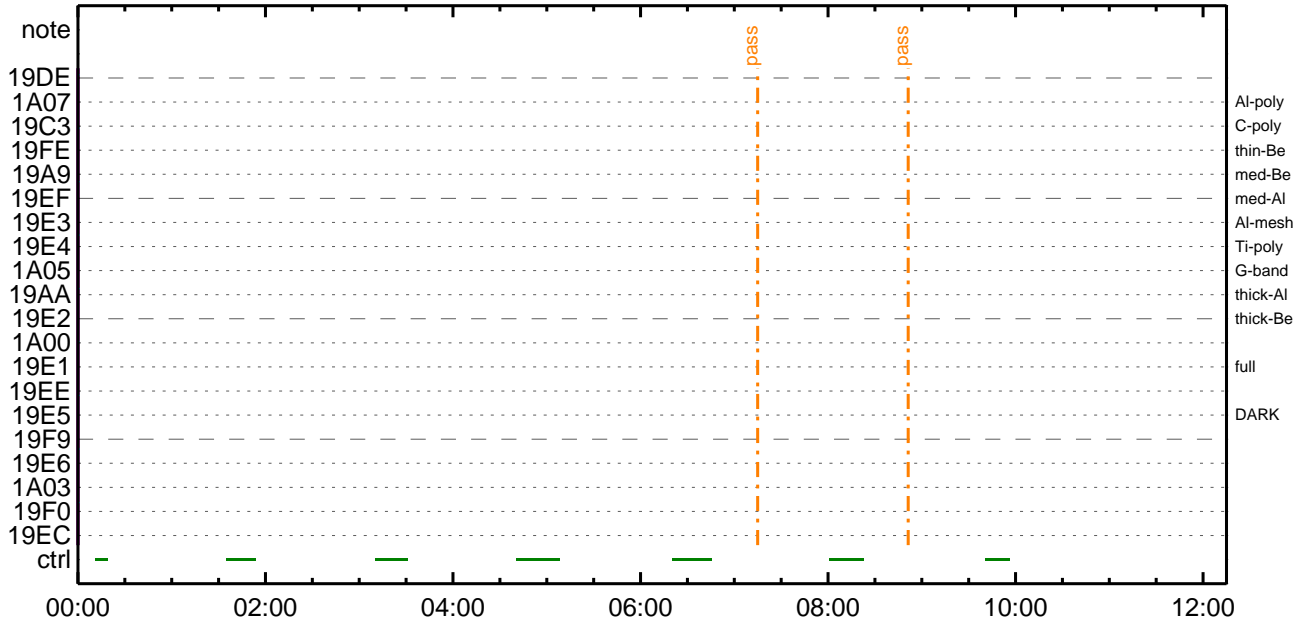
CMDI #0189 2014/04/03



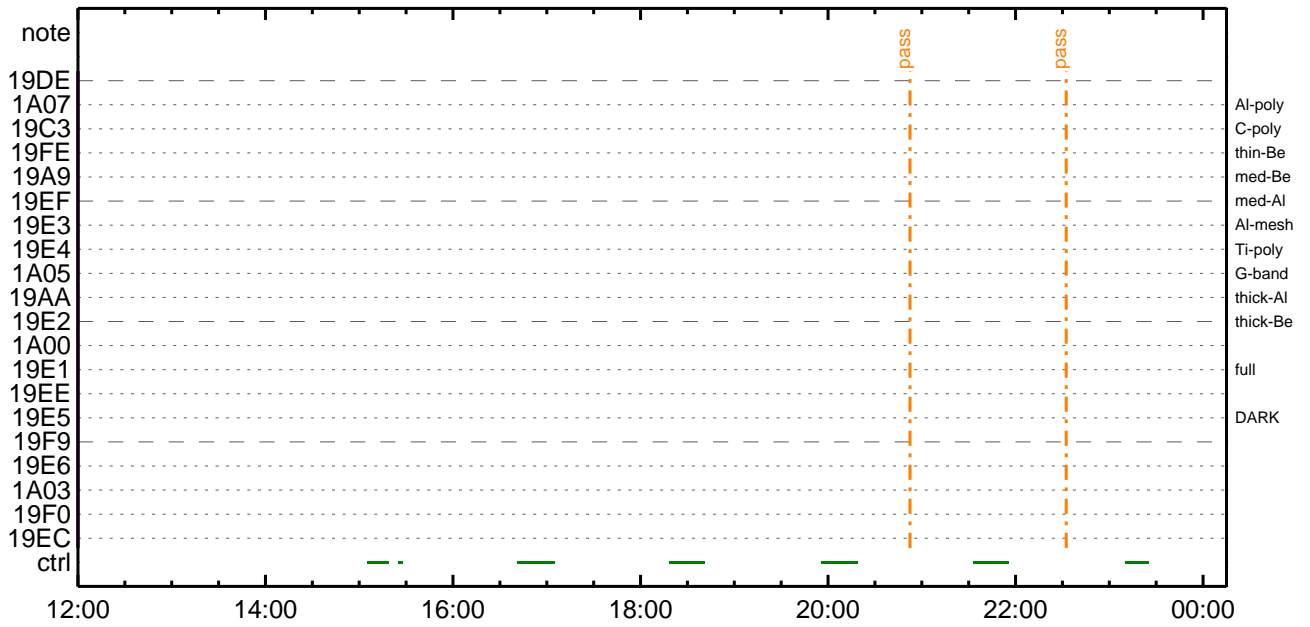
CMDI #0189 2014/04/03



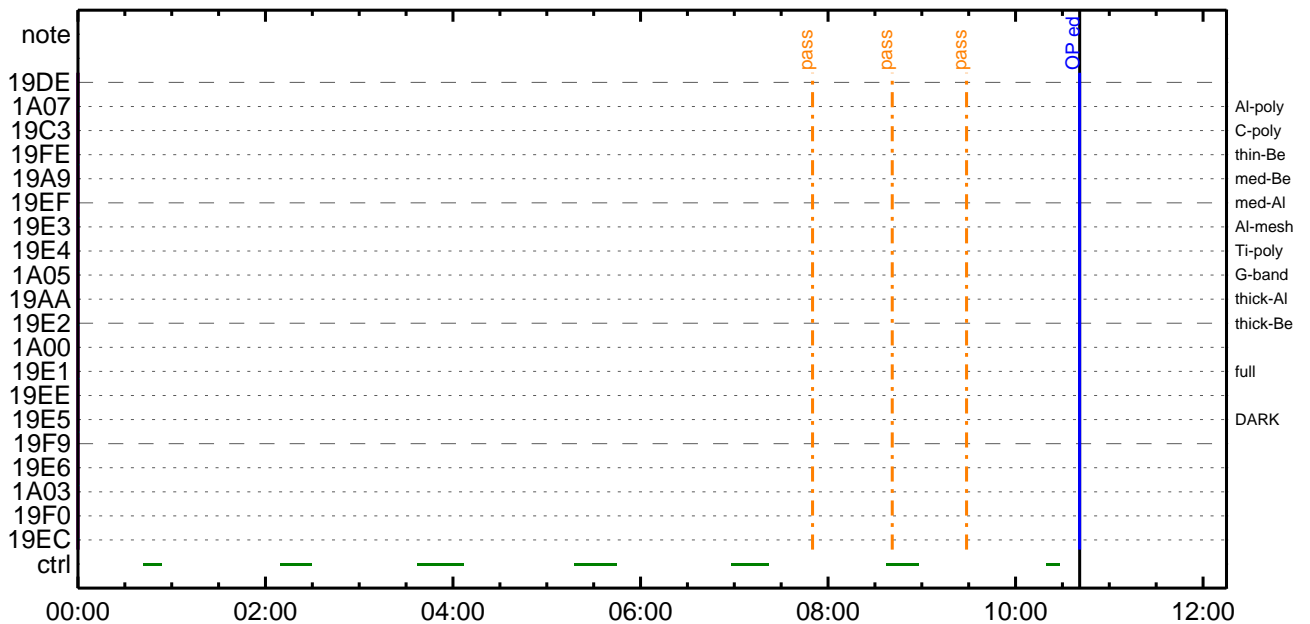
CMDI #0189 2014/04/04



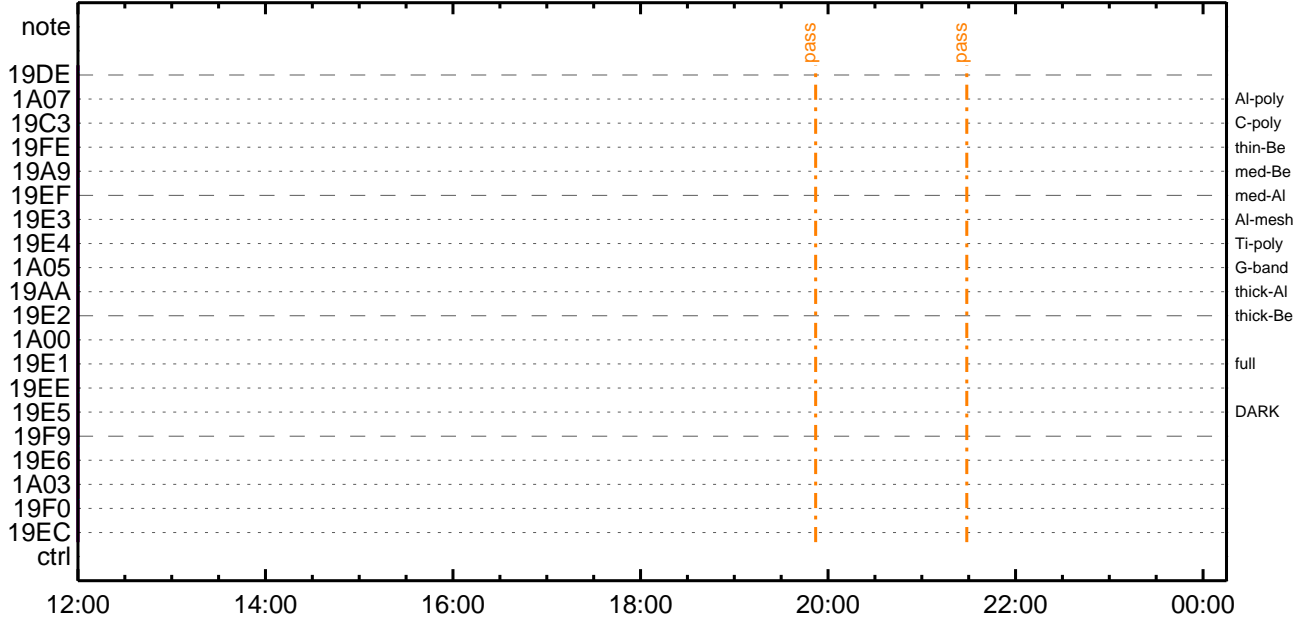
CMDI #0189 2014/04/04



CMDI #0189 2014/04/05



CMDI #0189 2014/04/05




```

0096 C.
0097 C.
0098 C. *****
0099 C. OP/OGY1;4YE;ã
0100 C. *****
0101 C.
0102 C. ;ãOP/OGY1;4YE;ã
0103 S. OP op-293:OP
0104 ( )
0105 S. OG og-293:OG
0106 ( )
0107 C.
0108 C. ;ãNMOG&OPîî°èYAYôYx;ã
0109 C. NMOG(0x200000-0x207FFF;§ 32 kbyte)
0110 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0111 BC (20 00 7f 01 02)
0112 C. çç[HK1_DMP_TOP_ADRS_1] EQ 40
0113 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0114 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0115 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0116 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0117 +. DC 01-22 DHU_MODE_CHNG
0118 BC (07 0b f8)
0119 C. çç[HK1_PKT_FORM_NO] EQ 7
0120 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0121 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0122 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0123 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0124 C. YAYôYx½ªî»ò³îÇ§
0125 C. çç[HK1_DMP_CHK_FLG] EQ NON
0126 C. RAM ID=NMOG²î½E¹ç•è²îOK²³îÇ§
0127 C.
0128 C. NMOG(0x208000-0x20FFFF;§ 32 kbyte)
0129 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0130 BC (20 80 7f 01 02)
0131 C. çç[HK1_DMP_TOP_ADRS_1] EQ 41
0132 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0133 C. çç[HK1_DMP_BLOCK_NUM] EQ 127
0134 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0135 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0136 +. DC 01-22 DHU_MODE_CHNG
0137 BC (07 0b f8)
0138 C. çç[HK1_PKT_FORM_NO] EQ 7
0139 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0140 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0141 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0142 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0143 C. YAYôYx½ªî»ò³îÇ§
0144 C. çç[HK1_DMP_CHK_FLG] EQ NON
0145 C. RAM ID=NMOG²î½E¹ç•è²îOK²³îÇ§
0146 C.
0147 C. NMOG(0x210000-0x2100FF;§ 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)
0148 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0149 BC (21 00 41 01 02)
0150 C. çç[HK1_DMP_TOP_ADRS_1] EQ 42
0151 C. çç[HK1_DMP_TOP_ADRS_0] EQ 0
0152 C. çç[HK1_DMP_BLOCK_NUM] EQ 65
0153 C. çç[HK1_DMP_REPEAT_NUM] EQ 0
0154 C. çç[HK1_DMA_DMP_PIM] EQ DHU
0155 +. DC 01-22 DHU_MODE_CHNG
0156 BC (07 0b f8)
0157 C. çç[HK1_PKT_FORM_NO] EQ 7
0158 C. çç[HK1_PKT_GEN_TIME] EQ 0.25 s
0159 C. çç[HK1_S_TLM_BIT_RATE] EQ 32k
0160 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0161 C. çç[HK1_DMP_CHK_FLG] EQ EXEC
0162 C. YAYôYx½ªî»ò³îÇ§
0163 C. çç[HK1_DMP_CHK_FLG] EQ NON
0164 C. RAM ID=NMOG, RAM ID=OP²î½E¹ç•è²îOK²³îÇ§
0165 C.
0166 C. ***** °E²¼²î½E¹ç•è²îOK²³îÇ§ *****
0167 C. DHUYâ;4YE;E½Y½;Yi;4YE;E²òîã¹
0168 +. DC 01-22 DHU_MODE_CHNG
0169 BC (02 0a f8)
0170 C. çç[HK1_PKT_FORM_NO] EQ 2
0171 C. çç[HK1_PKT_GEN_TIME] EQ 0.5S
0172 C. çç[HK1_S_TLM_BIT_RATE] EQ 32K
0173 C. çç[HK1_X_TLM_BIT_RATE] EQ 4M
0174 C.
0175 C. *****
0176 C. TI-CMD SET (OPOG STOP/COPY/START)
0177 C. *****
0178 C.
0179 C. NOTICE ;§ OPOG UPLOAD²-Á÷ç@NG²î½E¹ç•è²îOK²³îÇ§
0180 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0181 C.
0182 C. TIY³Y½YôYx½ªî»ò³îÇ§ (UT)
0183 +. TI 2014-04-01 09:16:00.0
0184 DC 01-B3 DHU_OP_STOP
0185 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0186 C.
0187 +. TI 2014-04-01 09:16:01.0
0188 DC 01-B4 DHU_OP_COPY
0189 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP
0190 C.
0191 +. TI 2014-04-01 09:16:01.0
0192 DC 01-B5 DHU_OPOG_COPY
0193 C. çç[HK1_TI_CMD_NUM] EQ 1COUNTUP

```

```

0194 C.
0195 +. TI 2014-04-01 09:20:59.5
0196 DC 01-B2 DHU_OP_START
0197 C.      çç[HK1_TI_CMD_NUM]      EQ      1COUNTUP
0198 C.
0199 C. °Ê²¼œïÄë%îîñœîŷÄŷ§ŷÄŷ¹àîÛ
0200 C.      çç[HK1_TI_CMD_ENA/DIS]    EQ      ENA
0201 C.      çç[HK1_TI_CMD_NUM]      EQ      4
0202 C.      çç[HK1_NEXT_EXEC_PIM]    EQ      DHU
0203 C.      çç[HK1_NEXT_EXEC_DC]    EQ      0xB3
0204 C.
0205 C. *****
0206 C. TIîî°èŷÄŷÖŷ×
0207 C. *****
0208 C.
0209 C. TI_TBL(0x03AB00-0x03AEFF;§ 1024byte)
0210 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0211 BC      (03 ab 03 01 02)
0212 C.      çç[HK1_DMP_TOP_ADRS_1]  EQ      07
0213 C.      çç[HK1_DMP_TOP_ADRS_0]  EQ      2B
0214 C.      çç[HK1_DMP_BLOCK_NUM]    EQ      3
0215 C.      çç[HK1_DMP_REPEAT_NUM]  EQ      0
0216 C.      çç[HK1_DMA_DMP_PIM]     EQ      DHU
0217 +. DC 01-22 DHU_MODE_CHNG
0218 BC      (07 0b f8)
0219 C.      çç[HK1_PKT_FORM_NO]     EQ      7
0220 C.      çç[HK1_PKT_GEN_TIME]    EQ      0.25 s
0221 C.      çç[HK1_S_TLM_BIT_RATE]  EQ      32k
0222 C.      çç[HK1_X_TLM_BIT_RATE]  EQ      4M
0223 C.      çç[HK1_DMP_CHK_FLG]     EQ      EXEC
0224 C.
0225 C. ŷÄŷÖŷ×½ªî»œ³îç§
0226 C.      çç[HK1_DMP_CHK_FLG]     EQ      NON
0227 C.
0228 C. RAM ID=TI_TBLœîî°è¹ç•è²îœœ³îç§
0229 C.
0230 C. DHUŷä;¼ŷÉ;Ê¼ŷ¼.ŷî;¼ŷÉ;Êœðîäœ¹
0231 +. DC 01-22 DHU_MODE_CHNG
0232 BC      (02 0a f8)
0233 C.      çç[HK1_PKT_FORM_NO]     EQ      2
0234 C.      çç[HK1_PKT_GEN_TIME]    EQ      0.5S
0235 C.      çç[HK1_S_TLM_BIT_RATE]  EQ      32K
0236 C.      çç[HK1_X_TLM_BIT_RATE]  EQ      4M
0237 C.
0238 C.
0239 C. ***** XRT START *****
0240 C. Execute, after the success of OP upload.
0241 +. TI 2014-04-01 09:20:00.0
0242 DC 07-F0 MDP_XRT_MODE_STBY
0243 BC      (c3)
0244 C.      [      ] [HK1_TI_CMD_NUM] EQ      1COUNTUP
0245 C.
0246 C. ***** XRT END *****
0247 C. *****
0248 C. SOT TI command set
0249 C. *****
0250 C. Execute, after the success of OP upload.
0251 +. TI 2014-04-01 09:20:16.0
0252 DC 07-F0 MDP_SOT_MODE_STBY
0253 BC      (41)
0254 C. -----
0255 C. HK1_TI_CMD_NUM      = 1 CNTUP [      ]
0256 C. -----
0257 C. ***** SOT END *****
0258 C. Stop EIS observation and temporarily disable EIS mode changes
0259 C.
0260 C.
0261 C. ***** Start EIS operation (TI set) *****
0262 C. Execute, after the success of OP upload.
0263 C. Set EIS TI-commands
0264 +. TI 2014-04-01 09:20:30.0
0265 DC 07-FC EIS_MODE_MANU
0266 BC      (21 02)
0267 +. TI 2014-04-01 09:20:40.0
0268 DC 07-FC EIS_MODE_CHG_DIS
0269 BC      (22)
0270 C.      [      ] [HK1_TI_CMD_NUM] EQ      2 COUNTUP
0271 C. ***** End EIS operation (TI set) *****
0272 C.
0273 C.
0274 C.
0275 C. ***** MDP ´ûÄîœî»ö¼ŷœÊÄðœ¹œDCBC•x²è *****
0276 C. (¼ä°îŷÖŷÄŷÉŷŷŷÉŷáŷçŷèœ¼œœ¼Ä»Ûœ¹œè)
0277 S. DC-BC dcbc-402:DCBC
0278 (MDP_known_event)
0279 C.
0280 C.
0281 C. ***** ŷÐŷ¹•î Daily±çîñœÊ´œ¹œœDCBC•x²è *****
0282 S. DC-BC dcbc-153:DCBC
0283 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0284 C.
0285 C.
0286 C. ;ãLOSŷÄŷ§ŷÄŷ¹¼Ä»Û;ä
0287 C.
0288 C. ***** LOS *****
0289 C.

```


(a) Spacecraft Operation Procedure (real-commands)

```
main-295 2014-04-01 13:29:13 146 33 SOLAR-B MAIN //
0001 C.
0002 . C. ***** AOS *****
0003 C.
0004 . C. ;ãAOSYÁY$YÁY-¼Á»Û;ã
0005 C.
0006 C. YÁYB;¼Y³YF¥ÓYÉÁ+¿®
0007 +. DC 00-00 NULL_DUMMY_CMD
0008 C.
0009 . C. ***** AOCs : Reload orbital element (send every contact) *****
0010 C. Áí;Èø¿øÁø•µ°È»ÍxÁÇøíYçYÁY×Yí;¼YÉ;ÈÈè%µ•ííÉ;ÈøÈ¼°ÇÓø•ø¿¼í¹çøí;çÀ®, ùø¹øèøøøçÁ+¿®ø•øÈøøøøøÈ;f
0011 +. DC 02-8E AOCU_ORB_UPD
0012 C.
0013 C.
0014 C.
0015 C. ***** XRT START *****
0016 C.
0017 +. DC 07-F0 MDP_XRT_CTRL_MANU
0018 BC (c1)
0019 + DC 07-F0 MDP_XRT_MODE_STBY
0020 BC (c3)
0021 . C. ----- Success Verify ? OK / NG____
0022 C.
0023 C. XRT Obs. Table Upload
0024 . S. RAM ram-291:MDP_OBS_X
0025 ( )
0026 C.
0027 +. DC 07-F0 MDP_DUMP_XRTTBL
0028 BC (84 07 00 00 00 3a d4)
0029 . C. ----- Comparison Check ? OK / ERR ____
0030 C.
0031 C.
0032 +. DC 07-F0 MDP_XRT_ROI_SET
0033 BC (cd 01 b1 b1 04 04)
0034 + DC 07-F0 MDP_XRT_ROI_SET
0035 BC (cd 02 b1 b1 08 08)
0036 + DC 07-F0 MDP_XRT_ROI_SET
0037 BC (cd 03 b1 b1 08 08)
0038 + DC 07-F0 MDP_XRT_ROI_SET
0039 BC (cd 04 b1 b1 06 06)
0040 + DC 07-F0 MDP_XRT_ROI_SET
0041 BC (cd 05 85 83 06 06)
0042 + DC 07-F0 MDP_XRT_ROI_SET
0043 BC (cd 06 85 83 06 06)
0044 + DC 07-F0 MDP_XRT_ROI_SET
0045 BC (cd 0f 80 80 06 06)
0046 + DC 07-F0 MDP_XRT_ROI_SET
0047 BC (cd 10 80 80 08 08)
0048 + DC 07-F0 MDP_XRT_FLD_ENA
0049 BC (d8)
0050 + DC 07-F0 MDP_XRT_FLRCTRL_ENA
0051 BC (c8)
0052 + DC 07-F0 MDP_XRT_AEC_RESET
0053 BC (d0)
0054 + DC 07-F0 MDP_XRT_ARS_DIS
0055 BC (d5)
0056 + DC 07-F0 MDP_XRT_FLD_RESET
0057 BC (da)
0058 +. DC 07-F0 MDP_XRT_QT_PROG_SET
0059 BC (c4 07)
0060 +. DC 07-F0 MDP_XRT_QT_PROG_SET
0061 BC (c4 02)
0062 . C. ----- Success Verify ? OK / NG ____
0063 C.
0064 C.
0065 . C. All OK? Yes--> Please Proceed. / No --> Stop here.
0066 C.
0067 +. DC 07-F0 MDP_XRT_MODE_OBSV
0068 BC (c2)
0069 +. TI 2014-04-01 09:20:02.0
0070 DC 07-F0 MDP_XRT_MODE_OBSV
0071 BC (c2)
0072 . C. ----- Success Verify ? OK / NG ____
0073 C.
0074 C. ***** XRT END *****
0075 . C. *****
0076 C. SOT table upload
0077 C. *****
0078 . C. < Stop FG table >
0079 +. DC 07-F0 MDP_FG_CTRL_MANU
0080 BC (51)
0081 . C. -----
0082 C. MDP_FG_CTRL_MODE = MANU [ ]
0083 C. -----
0084 C.
0085 . C. <Upload FG Observation Table>
0086 . S. RAM ram-266:MDP_OBS_F
0087 ( )
0088 C.
0089 . C. < Dump RAMID=MDP_OBS_F >
0090 +. DC 07-F0 MDP_DUMP_FGTBL
0091 BC (82 07 00 00 00 38 b8)
0092 C. -----
0093 C. MDP_OBS_F verify = OK/NG [ ]
0094 C. -----
0095 C.
```

```
0096 . C. < Upload DPL table >
0097 C.
0098 C.  YcYÅYxYí;¼YÉoîÁ°oËESTS_CHKoðOFFoËo¹oë
0099 C.
0100 . S. RAM   ram-271:MDP_DPL
0101  ( )
0102 C.
0103 . C. < Dump RAMID=MDP_DPL >
0104 +. DC 07-F0 MDP_DUMP_FGTBL
0105 BC   (82 07 00 38 b8 00 40)
0106 C. -----
0107 C.   MDP_DPL verify         = OK    [ ]
0108 C. -----
0109 C.
0110 C.   STS_CHKoðONoËo¹oë
0111 C.
0112 . C. < Update MDP DSC PAR1 >
0113 +. DC 07-F0 MDP_DSC_PAR1_UPDATE
0114 BC   (4c)
0115 C.   MDP_CMD_CODE          = F04C0700[ ]
0116 C.   MDP_CMD_CNT           (count-up 1) [ ]
0117 C. -----
0118 C.
0119 . C.
0120 C. *****
0121 C.   SOT TI command set
0122 C. *****
0123 C. Execute, after the success of TBL upload.
0124 +. TI 2014-04-01 09:20:18.0
0125 DC 07-F0 MDP_SOT_MODE_OBSV
0126 BC   (40)
0127 . C. -----
0128 C.   HK1_TI_CMD_NUM         = 1 CNTUP [ ]
0129 C. -----
0130 C.
0131 C.
0132 . C. ***** MDP  ´ûÃîoî»ö¼Y°ÊÄo¹oëDCBC•x²è *****
0133 C. (¼Á°îYÓYÅYÈYÞYËYÁYçYèoË¼o¼Â»Ûo¹oë)
0134 . S. DC-BC dcbc-402:DCBC
0135       (MDP_known_event)
0136 C.
0137 C.
0138 . C. ***** YDÝ¹·Ī Daily±¿ĪÑoË´Øo¹oëDCBC•x²è *****
0139 . S. DC-BC dcbc-153:DCBC
0140       (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0141 C.
0142 C.
0143 . C.  ¦ãLOS¥Á¥$¥Ã¥~¼Â»Û;ã
0144 C.
0145 . C. ***** LOS *****
0146 C.
```

*** OP Sequence for XRT ***

```

2014/04/01 09:29:30.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 09:29:32.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 09:29:34.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 09:31:00.0 AOCS_Ore-point_Start_1_OG [0x097]
                        AOCU_NM 5 02-76 03 00 00 00 00
2014/04/01 09:32:44.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 14:54:30.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 14:54:32.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 14:54:34.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 14:57:44.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 16:30:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 16:30:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 16:30:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 16:33:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 18:07:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 18:07:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 18:07:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 18:10:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 19:44:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 19:44:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 19:44:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 19:47:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 21:21:30.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 21:21:32.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 21:21:34.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 21:24:44.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 22:59:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/01 22:59:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/01 22:59:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/01 23:02:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/01 23:30:00.0 AOCS_Ore-point_Start_2_OG [0x098]
                        AOCU_NM 5 02-76 00 ef e0 af 54
2014/04/02 00:36:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/02 00:36:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/02 00:36:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/02 00:39:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/02 01:58:30.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/02 01:58:32.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/02 01:58:34.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/02 02:01:44.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/02 03:29:30.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/02 03:29:32.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/02 03:29:34.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/02 03:32:44.0 XRT_PREFLR_STOP_419_OG [0x1a3]
                        MDP_XRT_PREFLR_STOP 1 07-F0 e9
2014/04/02 05:06:00.0 XRT_CTRL_MANU_400_OG [0x190]
                        MDP_XRT_CTRL_MANU 1 07-F0 c1
2014/04/02 05:06:02.0 XRT_FLD_RESET_415_OG [0x19f]
                        MDP_XRT_FLD_RESET 1 07-F0 da
2014/04/02 05:06:04.0 XRT_PREFLR_STRT_418_OG [0x1a2]
                        MDP_XRT_PREFLR_STRT 1 07-F0 e8
2014/04/02 05:09:14.0 XRT_PREFLR_STOP_419_OG [0x1a3]

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2014/04/02	06:00:00.0	AOCS_ORe-point_Start_3_OG [0x099]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
		AOCU_NM		5	02-76	00 00 00 00 00	
2014/04/02	06:10:00.0	AOCS_ORe-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	00 ef e0 af 54	
2014/04/02	06:46:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	06:46:32.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	06:46:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	06:49:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	08:26:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	08:26:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	08:26:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	08:29:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	10:07:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	10:07:32.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	10:07:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	10:10:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	12:00:00.0	AOCS_ORe-point_Start_4_OG [0x09a]	AOCU_NM	5	02-76	00 ff 1b ad 82	
2014/04/02	13:58:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	13:58:32.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	13:58:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	14:00:00.0	AOCS_ORe-point_Start_5_OG [0x09b]	AOCU_NM	5	02-76	02 00 00 00 00	
2014/04/02	14:01:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	15:30:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	15:30:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	15:30:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	15:33:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	17:06:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	17:06:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	17:06:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	17:09:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	18:43:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	18:43:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	18:43:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	18:46:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	20:00:00.0	AOCS_ORe-point_Start_2_OG [0x098]	AOCU_NM	5	02-76	00 ef e0 af 54	
2014/04/02	20:20:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	20:20:32.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	20:20:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	20:23:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	21:58:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	21:58:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	21:58:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	22:01:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/02	23:35:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/04/02	23:35:02.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/04/02	23:35:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/04/02	23:38:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/04/03	01:01:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_MANU	1	07-F0	c1	

2014/04/03	01:01:32.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	01:01:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	01:04:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	02:34:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2014/04/03	02:34:02.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	02:34:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	02:37:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	04:03:00.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2014/04/03	04:03:02.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	04:03:04.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	04:06:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	05:43:30.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2014/04/03	05:43:32.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	05:43:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	05:46:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	06:19:30.0	AOCS_ORe-point_Start_3_OG [0x099]							
		AOCU_NM	5	02-76	00 00 00 00 00				
2014/04/03	06:21:30.0	XRT_TCIB_XRT_S_HTR_A_DIS_437_OG [0x1b5]							
		TCIB_XRT_S_HTR_A_DIS	0	04-C0					
2014/04/03	06:29:30.0	AOCS_ORe-point_Start_3_OG [0x099]							
		AOCU_NM	5	02-76	00 00 00 00 00				
2014/04/03	07:23:30.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2014/04/03	07:23:32.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	07:23:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	07:26:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	09:03:30.0	XRT_CTRL_MANU_400_OG [0x190]							
		MDP_XRT_CTRL_MANU	1	07-F0	c1				
2014/04/03	09:03:32.0	XRT_FLD_RESET_415_OG [0x19f]							
		MDP_XRT_FLD_RESET	1	07-F0	da				
2014/04/03	09:03:34.0	XRT_PREFLR_STRT_418_OG [0x1a2]							
		MDP_XRT_PREFLR_STRT	1	07-F0	e8				
2014/04/03	09:06:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]							
		MDP_XRT_PREFLR_STOP	1	07-F0	e9				
2014/04/03	09:30:00.0	AOCS_ORe-point_Start_2_OG [0x098]							
		AOCU_NM	5	02-76	00 ef e0 af 54				
2014/04/03	11:16:00.0	AOCS_ORe-point_Start_3_OG [0x099]							
		AOCU_NM	5	02-76	00 00 00 00 00				