

# XRT Timeline to be uploaded on 2014/10/30

Period: 2014/10/30 10:19:00 - 2014/11/04 09:17:00

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Normal mode

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## XOB #19E6: AR Standard-A(Filter-Ratio with Al/poly and thin-Be) with PFB, 384x384 at 1064 1048, thin-Be, thick-Al, and Al/Poly context, with G-band (33ms)

Term	Pointing (x, y)	Comment
10/30 10:32:00 - 10/30 12:00:00	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)
10/30 15:03:06 - 10/30 17:55:54	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)
10/30 18:09:00 - 10/31 06:28:24	Fixed ( 889.0, -275.0)	# AR 12192 cont.

PROG= 13 Inf.-time(s)

- Subr= 1 1-time(s) 2.0sec
  - Seqn= 8 2-time(s) 2.0sec
    - Open/G-band Open/G-band close Safe Norm 44ms Obs 1x1 384x384 (1064, 1048) DPCM 0 0 2.0sec
- Subr= 2 2-time(s) 2.0sec
  - Seqn= 24 1-time(s) 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 16.0s Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
    - Open/G-band Open/G-band open Safe Norm 32ms Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
  - Seqn= 42 4-time(s) 2.0sec
    - Al-poly/Open thin-Be/Open close Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 5.66s Obs 1x1 512x512 (1064, 1048) Q=95 3 0 2.0sec
    - Open/thick-Al Open/thick-Al close Safe Norm 16.0s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
  - Seqn= 62 8-time(s) 270.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.00s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
    - Al-poly/Open thin-Be/Open close Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 0 2.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.00s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 2.0sec
    - Al-poly/Open thin-Be/Open close Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 1 2.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.00s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 2.0sec
    - Al-poly/Open thin-Be/Open close Safe Norm 500ms Obs 1x1 384x384 (1064, 1048) Q=95 3 2 2.0sec

Default Filter Thicker Filter VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

## XOB #1A56: HOP244 - High cadence (30s thin-Be only) 384x384 at 1064 1048 with PFB

Term	Pointing (x, y)	Comment
10/30 12:03:06 - 10/30 15:00:00	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)

PROG= 04 Inf.-time(s)

- Subr= 1 1-time(s) 2.0sec
  - Seqn= 51 1-time(s) 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 16.0s Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
    - Open/G-band Open/G-band open Safe Norm 44ms Obs 1x1 384x384 (1064, 1048) Q=98 0 0 2.0sec
  - Seqn= 90 1-time(s) 2.0sec
    - Open/G-band Open/G-band close Safe Norm 63ms Obs 1x1 384x384 (1064, 1048) DPCM 0 0 2.0sec
- Subr= 2 1-time(s) 2.0sec
  - Seqn= 69 120-time(s) 15.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 0 6.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 1 6.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 2 6.0sec
    - thin-Be/Open med-Be/Open close Safe Norm 1.41s Obs 1x1 384x384 (1064, 1048) Q=95 3 3 6.0sec

Default Filter Thicker Filter VLS mode image Exp. CCD Bin ROI: size (center) Comp. AEC Buffer Interval

## XOB #1A53: Synoptic Q95 2x2 - Al/mesh(3/128/1024) + Dark cal(2x2 4x4 8x8 512 Q98) + Dark cal(1x1 512x2048 - 1x1 2048x512) + Ti-poly(16/362/2048) + Thin-Be

Term	Pointing (x, y)	Comment
10/30 17:59:00 - 10/30 18:05:54	Fixed ( 0.0, 0.0)	synoptic, shifted -4.0 min
10/31 06:31:30 - 10/31 06:39:00	Fixed ( 0.0, 0.0)	synoptic, shifted 28.5 min
10/31 07:56:30 - 10/31 08:09:30	Fixed ( 889.0, -275.0)	# AR 12192 AR cont. (HOP265 08-12UT)

PROG= 05 1-time(s)

- Subr= 1 1-time(s) 12.0sec
  - Seqn= 9 1-time(s) 4.0sec
    - Open/Al-mesh Open/Al-mesh close Safe Norm 3ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - Open/Al-mesh Open/Al-mesh close Safe Norm 125ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - Open/Al-mesh Open/Al-mesh close Safe Norm 1.00s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
  - Seqn= 5 1-time(s) 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 2x2 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 4x4 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 8x8 2048x2048 (1024, 1024) Q=98 0 0 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 1x1 2048x512 (1024, 1024) DPCM 0 0 2.0sec
    - Open/Ti-poly Open/thick-Al close Safe Dark 500ms Obs 1x1 512x2048 (1024, 1024) DPCM 0 0 2.0sec
  - Seqn= 40 1-time(s) 4.0sec
    - Open/Ti-poly Open/Ti-poly close Safe Norm 16ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - Open/Ti-poly Open/Ti-poly close Safe Norm 354ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - Open/Ti-poly Open/Ti-poly close Safe Norm 2.00s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
  - Seqn= 92 1-time(s) 2.0sec
    - thin-Be/Open thin-Be/Open close Safe Norm 32ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - thin-Be/Open thin-Be/Open close Safe Norm 500ms Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
    - thin-Be/Open thin-Be/Open close Safe Norm 4.00s Obs 2x2 2048x2048 (1024, 1024) Q=95 0 0 2.0sec
  - Seqn= 6 1-time(s) 2.0sec
    - Open/G-band Open/G-band open Safe Norm 8ms Obs 2x2 2048x2048 (1024, 1024) Q=90 0 0 2.0sec
    - Open/G-band Open/G-band close Safe Norm 32ms Obs 1x1 2048x2048 (1024, 1024) Q=95 0 0 2.0sec

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### Flare mode

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Term	Pointing (x, y)	Comment
10/30 10:32:00 - 10/30 12:00:00	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)
10/30 12:03:06 - 10/30 15:00:00	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)
10/30 15:03:06 - 10/30 17:55:54	Fixed ( 889.0, -275.0)	# OP start + 10min AR 12192 fixed pointing (HOP244 12UT-15UT)
10/30 18:09:00 - 10/31 06:28:24	Fixed ( 889.0, -275.0)	# AR 12192 cont.

**PROG= 01 30-time(s)**

<b>Subr= 1 30-time(s) 2.0sec</b>												
└ <b>Seqn= 26 1-time(s) 4.0sec</b>												
└ thin-Be/Open	med-Be/Open	close	Safe	Norm	8ms	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└ med-Be/Open	Open/thick-Al	close	Safe	Norm	250ms	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└ Open/thick-Al	Open/thick-Be	close	Safe	Norm	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
<b>Subr= 2 1-time(s) 2.0sec</b>												
└ <b>Seqn= 10 1-time(s) 2.0sec</b>												
└ med-Al/Open	med-Al/thick-Al	close	Safe	Norm	500ms	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└ Open/thick-Be	Open/thick-Be	close	Safe	Norm	2.00s	Obs	1x1	384x384 (1024, 1024)	Q=95	3	0	2.0sec
└ <b>Seqn= 11 1-time(s) 2.0sec</b>												
└ Al-poly/Open	Al-poly/thick-Al	close	Safe	Norm	125ms	Obs	2x2	512x512 (1024, 1024)	Q=95	2	0	2.0sec
└ <b>Seqn= 15 1-time(s) 2.0sec</b>												
└ Open/G-band	Open/G-band	open	Safe	Norm	44ms	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
└ Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	1x1	384x384 (1024, 1024)	Q=98	0	0	2.0sec
└ Open/thick-Al	Open/thick-Al	close	Safe	Dark	1.00s	Obs	2x2	512x512 (1024, 1024)	Q=98	0	0	2.0sec

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### Active Region Search

\* \* \* \* \*

NOT USED

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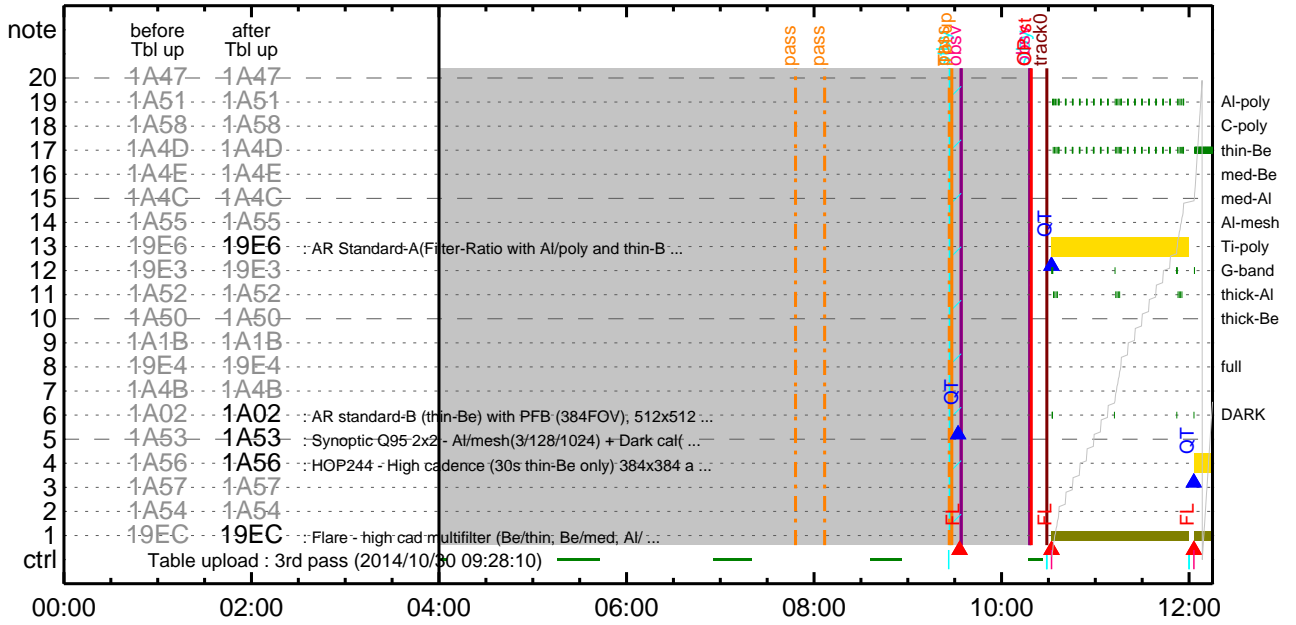
### Flare Detection

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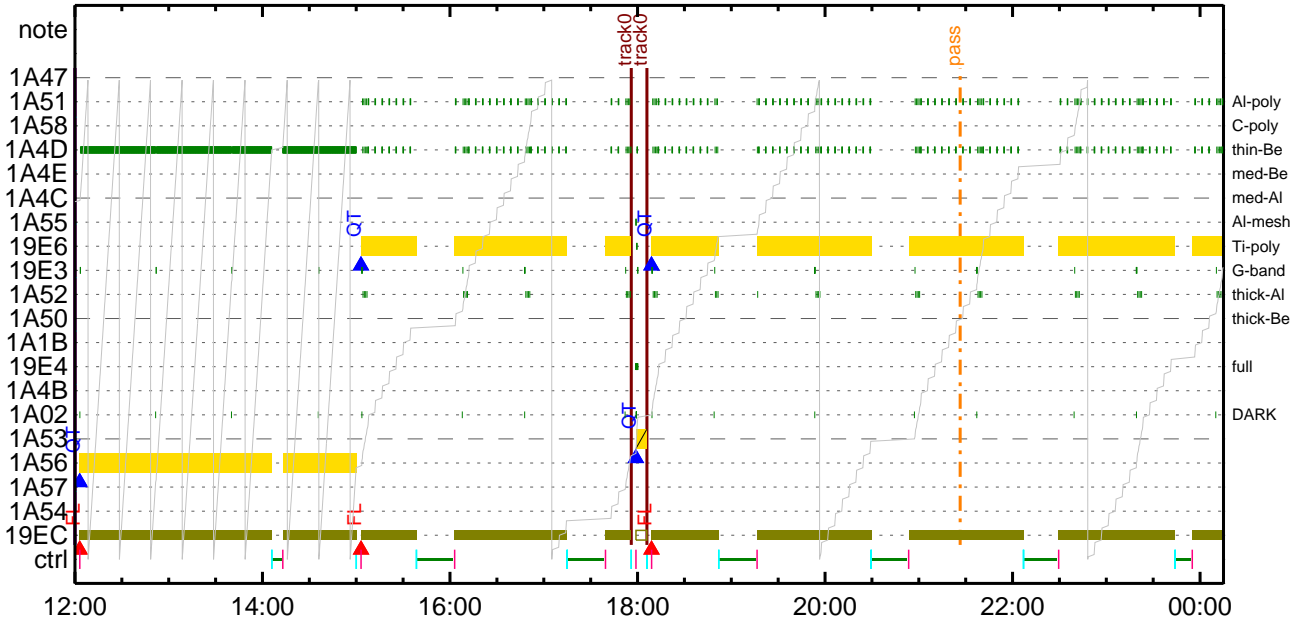
Term	Pointing (x, y)	Comment
10/30 18:06:18 - 10/31 06:28:48	Fixed ( 889.0, -275.0)	# AR 12192 cont.
Open/Ti-poly	Open/thick-Al	close Safe Norm 8ms Obs 8x8 Q=50 80sec

Default Filter	Thicker Filter	VLS	mode	image	Exp.	CCD	Bin	ROI: size (center)	Comp.	AEC Buffer	Interval
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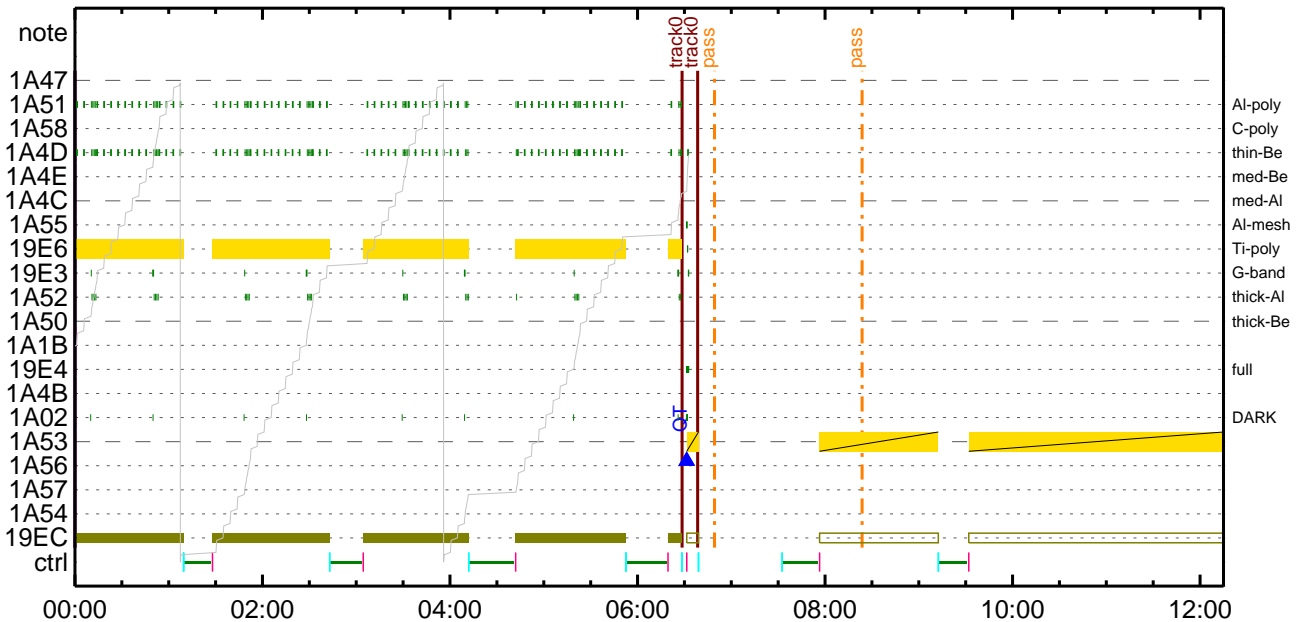
### CMDI #0680 2014/10/30



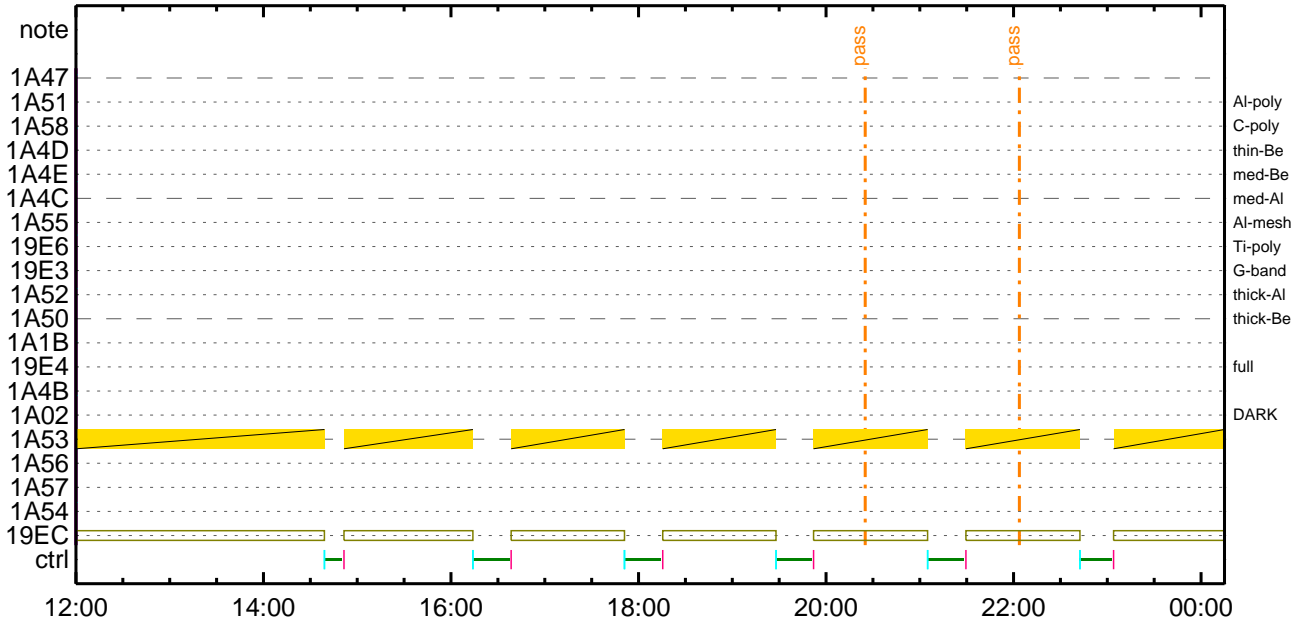
### CMDI #0680 2014/10/30



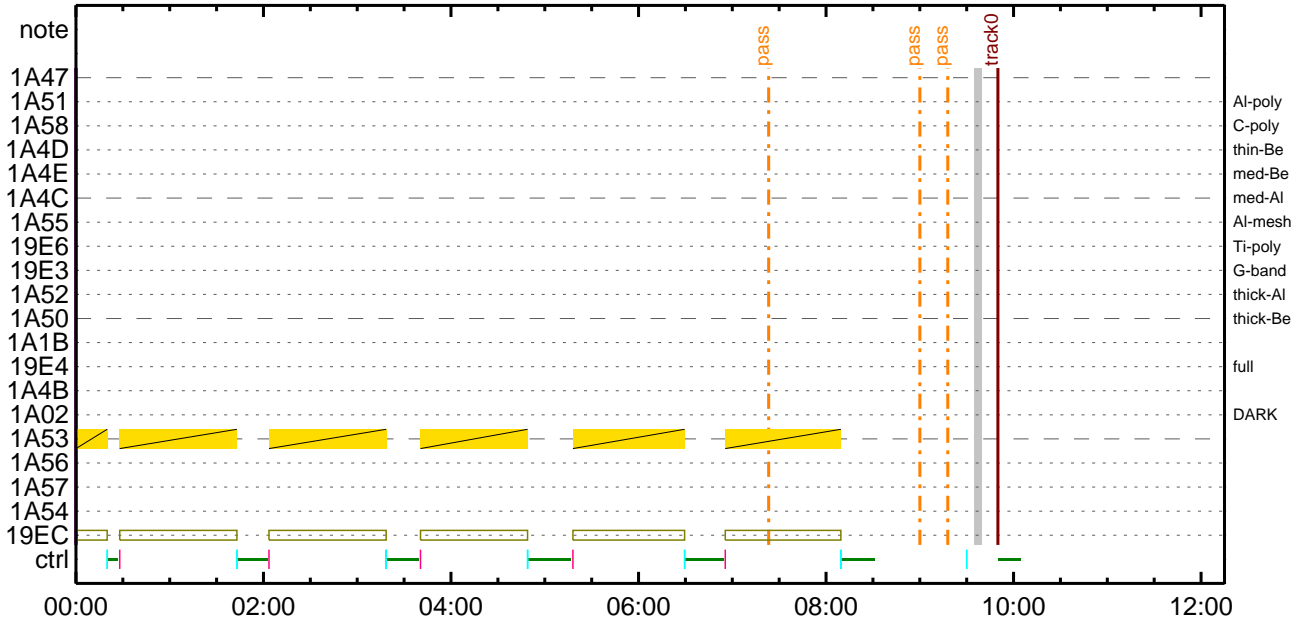
### CMDI #0680 2014/10/31



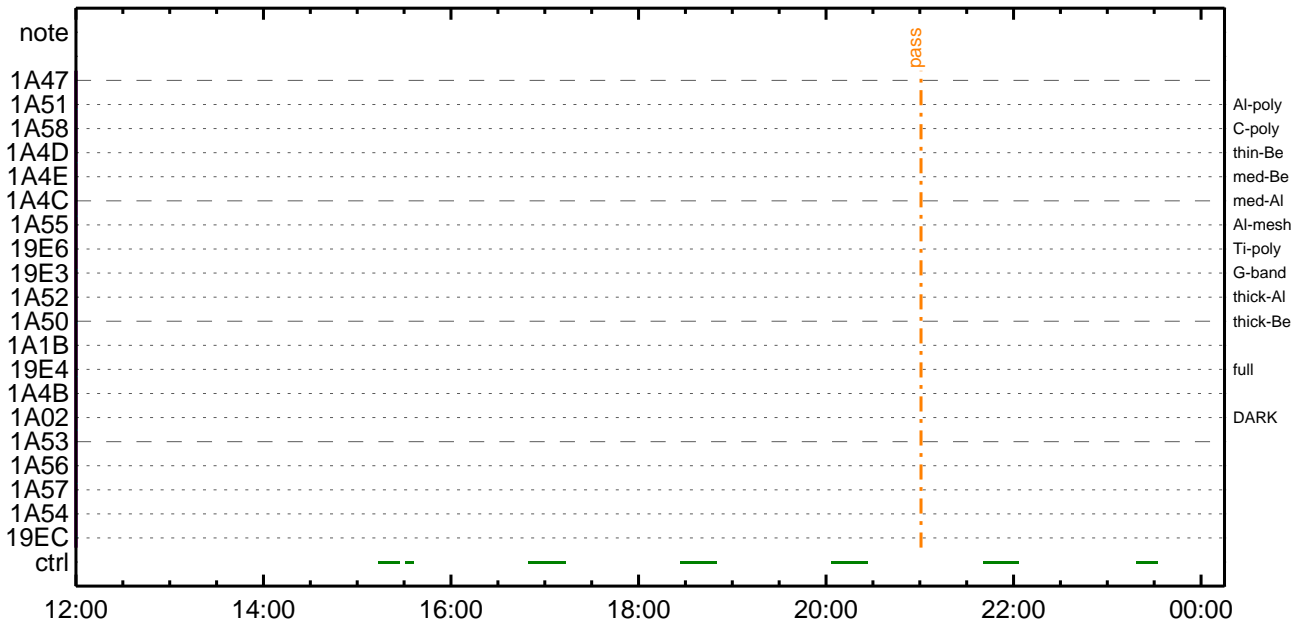
CMDI #0680 2014/10/31



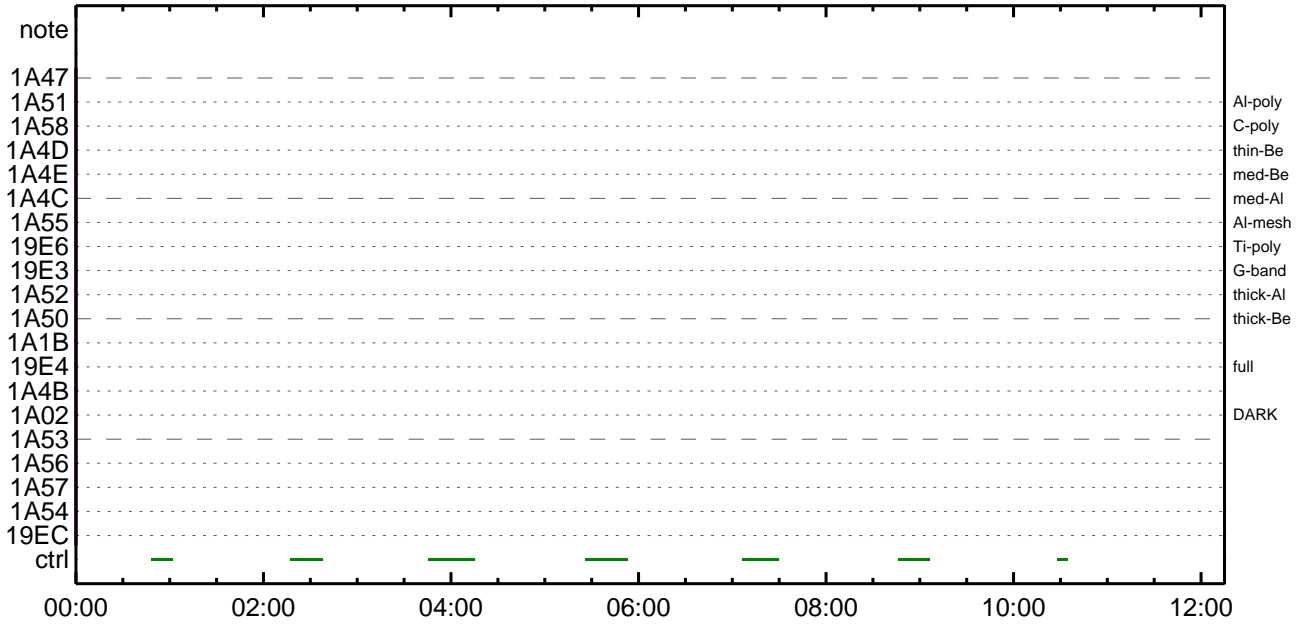
CMDI #0680 2014/11/01



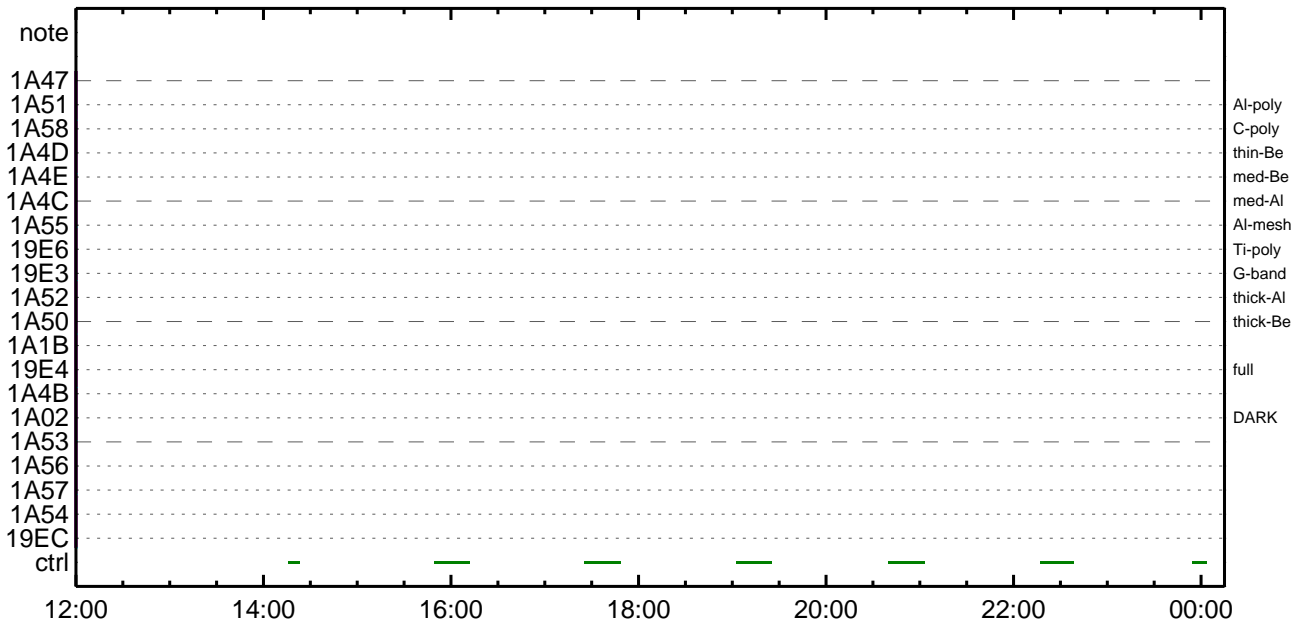
CMDI #0680 2014/11/01



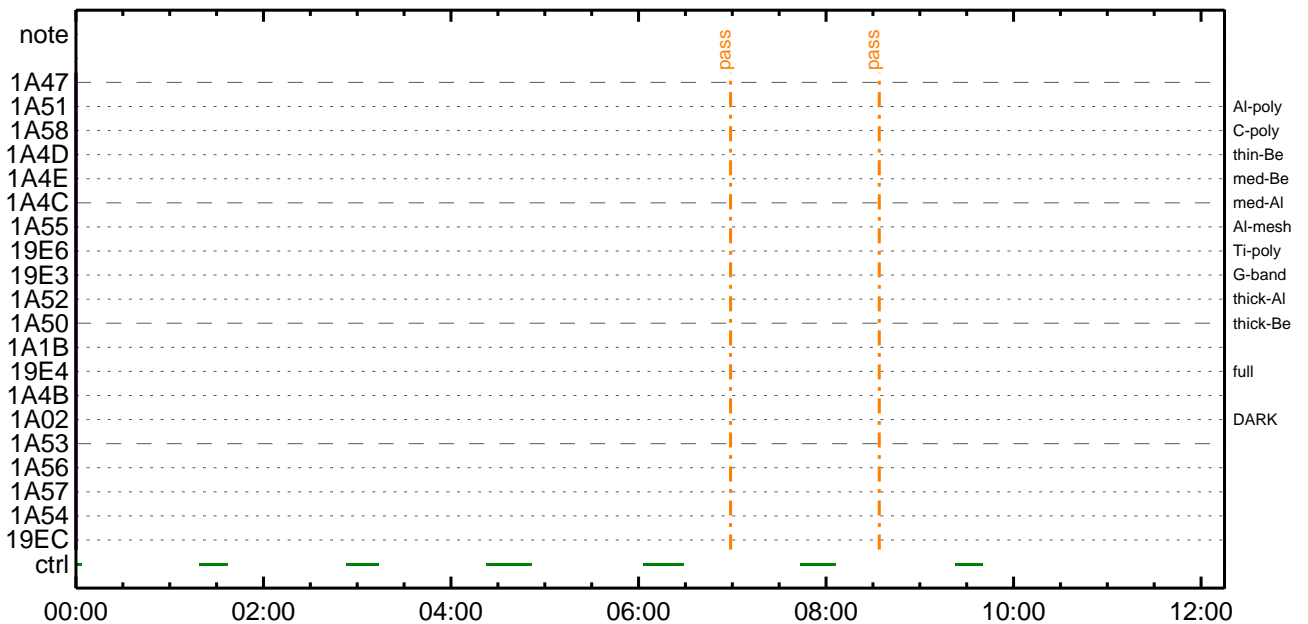
CMDI #0680 2014/11/02



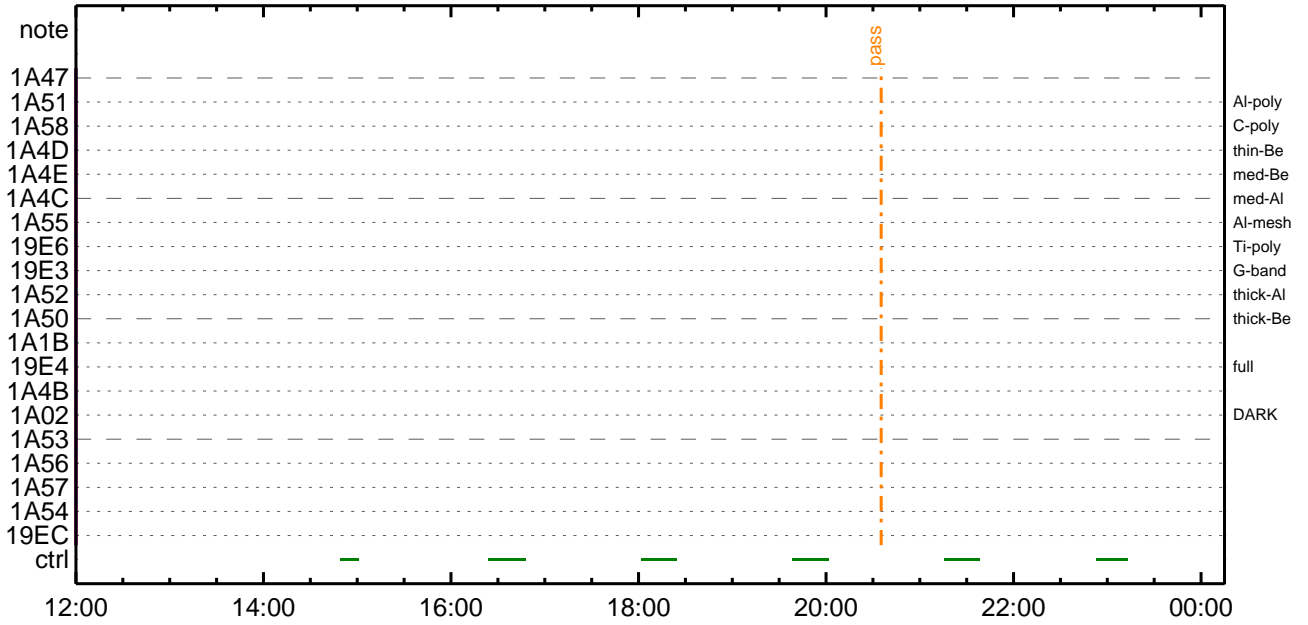
CMDI #0680 2014/11/02



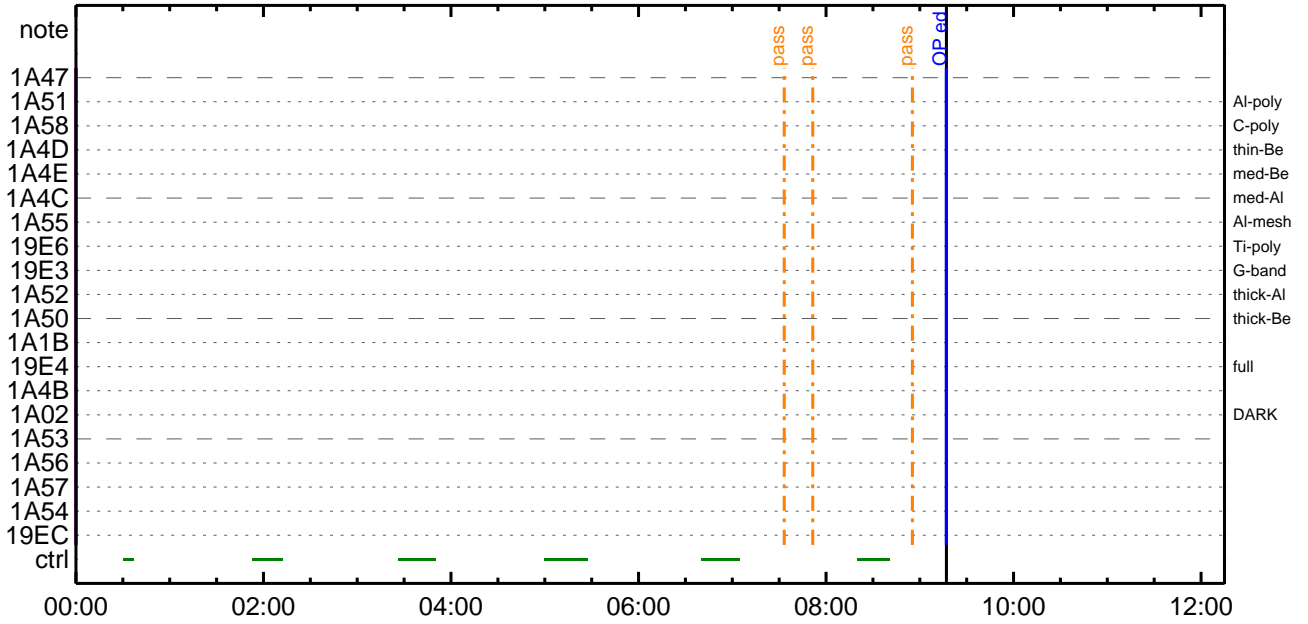
CMDI #0680 2014/11/03



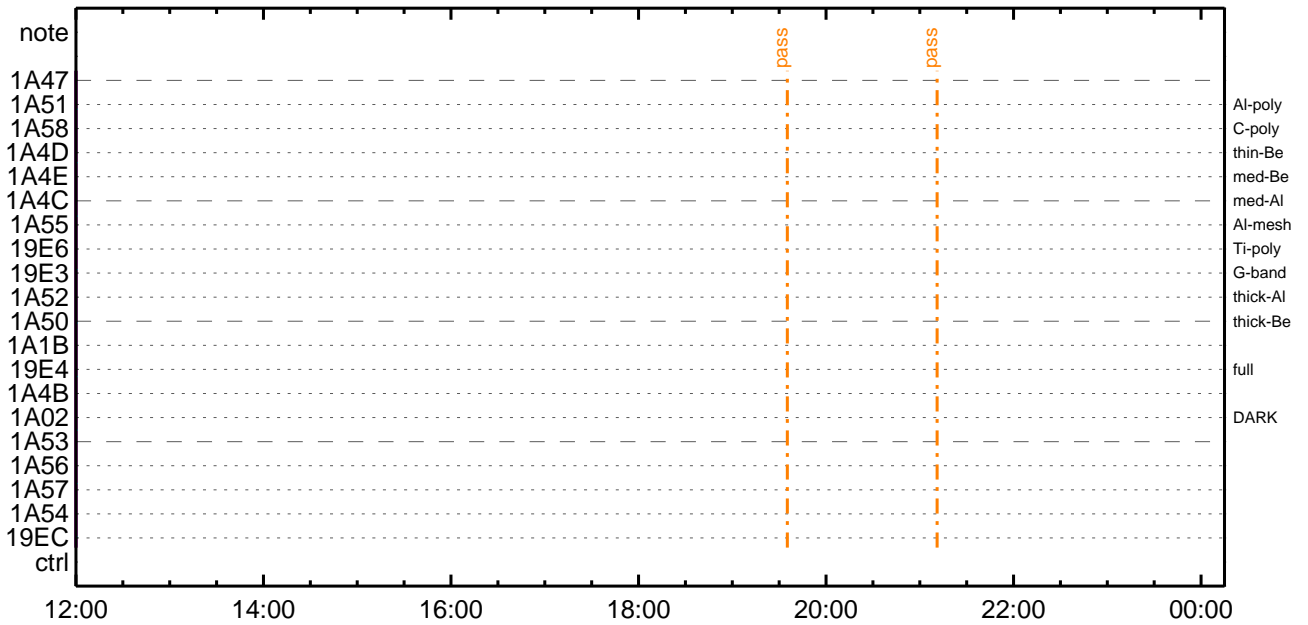
CMDI #0680 2014/11/03



CMDI #0680 2014/11/04



CMDI #0680 2014/11/04





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0096 C.
0097 C.
0098 C. *****
0099 C. OP/OGY1;4YE;ã
0100 C. *****
0101 C.
0102 . C. ;ãOP/OGY1;4YE;ã
0103 . S. OP   op-724:OP
0104   ( )
0105 . S. OG   og-724:OG
0106   ( )
0107 C.
0108 . C. ;ãNMOG&OPîî°è¥ÅYôYx;ã
0109 C. NMOG(0x200000-0x207FFF;§ 32 kbyte)
0110 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0111 BC   (20 00 7f 01 02)
0112 C.                   çç[HK1_DMP_TOP_ADRS_1]           EQ      40
0113 C.                   çç[HK1_DMP_TOP_ADRS_0]           EQ      0
0114 C.                   çç[HK1_DMP_BLOCK_NUM]            EQ     127
0115 C.                   çç[HK1_DMP_REPEAT_NUM]           EQ      0
0116 C.                   çç[HK1_DMA_DMP_PIM]               EQ     DHU
0117 +. DC 01-22 DHU_MODE_CHNG
0118 BC   (07 0b f8)
0119 C.                   çç[HK1_PKT_FORM_NO]               EQ      7
0120 C.                   çç[HK1_PKT_GEN_TIME]              EQ     0.25 s
0121 C.                   çç[HK1_S_TLM_BIT_RATE]            EQ     32k
0122 C.                   çç[HK1_X_TLM_BIT_RATE]            EQ      4M
0123 C.                   çç[HK1_DMP_CHK_FLG]               EQ     EXEC
0124 . C.   ¥ÅYôYx½ªî»ð³îÇ§
0125 C.                   çç[HK1_DMP_CHK_FLG]               EQ     NON
0126 . C. RAM ID=NMOGαî¼Ê¹ç•é²îOKαð³îÇ§
0127 C.
0128 C. NMOG(0x208000-0x20FFFF;§ 32 kbyte)
0129 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0130 BC   (20 80 7f 01 02)
0131 C.                   çç[HK1_DMP_TOP_ADRS_1]           EQ     41
0132 C.                   çç[HK1_DMP_TOP_ADRS_0]           EQ      0
0133 C.                   çç[HK1_DMP_BLOCK_NUM]            EQ     127
0134 C.                   çç[HK1_DMP_REPEAT_NUM]           EQ      0
0135 C.                   çç[HK1_DMA_DMP_PIM]               EQ     DHU
0136 +. DC 01-22 DHU_MODE_CHNG
0137 BC   (07 0b f8)
0138 C.                   çç[HK1_PKT_FORM_NO]               EQ      7
0139 C.                   çç[HK1_PKT_GEN_TIME]              EQ     0.25 s
0140 C.                   çç[HK1_S_TLM_BIT_RATE]            EQ     32k
0141 C.                   çç[HK1_X_TLM_BIT_RATE]            EQ      4M
0142 C.                   çç[HK1_DMP_CHK_FLG]               EQ     EXEC
0143 . C.   ¥ÅYôYx½ªî»ð³îÇ§
0144 C.                   çç[HK1_DMP_CHK_FLG]               EQ     NON
0145 . C. RAM ID=NMOGαî¼Ê¹ç•é²îOKαð³îÇ§
0146 C.
0147 C. NMOG(0x210000-0x2100FF;§ 256byte)+OP(0x210100-0x2141FF: 16.25kbyte)
0148 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0149 BC   (21 00 41 01 02)
0150 C.                   çç[HK1_DMP_TOP_ADRS_1]           EQ     42
0151 C.                   çç[HK1_DMP_TOP_ADRS_0]           EQ      0
0152 C.                   çç[HK1_DMP_BLOCK_NUM]            EQ     65
0153 C.                   çç[HK1_DMP_REPEAT_NUM]           EQ      0
0154 C.                   çç[HK1_DMA_DMP_PIM]               EQ     DHU
0155 +. DC 01-22 DHU_MODE_CHNG
0156 BC   (07 0b f8)
0157 C.                   çç[HK1_PKT_FORM_NO]               EQ      7
0158 C.                   çç[HK1_PKT_GEN_TIME]              EQ     0.25 s
0159 C.                   çç[HK1_S_TLM_BIT_RATE]            EQ     32k
0160 C.                   çç[HK1_X_TLM_BIT_RATE]            EQ      4M
0161 C.                   çç[HK1_DMP_CHK_FLG]               EQ     EXEC
0162 . C.   ¥ÅYôYx½ªî»ð³îÇ§
0163 C.                   çç[HK1_DMP_CHK_FLG]               EQ     NON
0164 . C. RAM ID=NMOG,RAM ID=OPαî¼Ê¹ç•é²îOKαð³îÇ§
0165 C.
0166 . C. ***** òÊ²¼αî¼Å´¶Ã°òÊÈ¬α°Ã÷ç® (¼âµ-¥ÅYôYx½ê¼çαðÃÔæαç¼ªα°°ðÊ¼ì¹çαçαâ) *****
0167 C. DHU¥â;¼¥Ê;Ê¼Y½;¥ì;¼¥Ê;Èαðîãα¹
0168 +. DC 01-22 DHU_MODE_CHNG
0169 BC   (02 0a f8)
0170 C.                   çç[HK1_PKT_FORM_NO]               EQ      2
0171 C.                   çç[HK1_PKT_GEN_TIME]              EQ     0.5S
0172 C.                   çç[HK1_S_TLM_BIT_RATE]            EQ     32K
0173 C.                   çç[HK1_X_TLM_BIT_RATE]            EQ      4M
0174 C.
0175 . C. *****
0176 C. TI-CMD SET (OPOG STOP/COPY/START)
0177 C. *****
0178 C.
0179 . C. NOTICE ; § OPOG UPLOADα¬Ã÷ç®NGuî¼î¹ç;ç°Ê²¼αîTI-CMDÃ÷ç®αî¼Å¹Ôα°αÊααα³αÊ;ç
0180 C.   α³αç;çSETαÊDUMPαîÆ±°ì¥N¥¹αç¹Ôα|α³αÊ;ç
0181 C.
0182 . C. TIY³¥P¥ôYÊαððÃîç(UT)
0183 +. TI 2014-10-30 10:14:00.0
0184 DC 01-B3 DHU_OP_STOP
0185 C.                   çç[HK1_TI_CMD_NUM]                 EQ     1COUNTUP
0186 C.
0187 +. TI 2014-10-30 10:14:01.0
0188 DC 01-B4 DHU_OP_COPY
0189 C.                   çç[HK1_TI_CMD_NUM]                 EQ     1COUNTUP
0190 C.
0191 +. TI 2014-10-30 10:14:01.0
0192 DC 01-B5 DHU_OPOG_COPY
0193 C.                   çç[HK1_TI_CMD_NUM]                 EQ     1COUNTUP

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0194 C.
0195 +. TI 2014-10-30 10:18:59.5
0196 DC 01-B2 DHU_OP_START
0197 C.          çç[HK1_TI_CMD_NUM]                      EQ      1COUNTUP
0198 C.
0199 C. °È²¼õİÄè%īīñõİŷÄŷ§ŷÄŷ-¹àİÜ
0200 C.          çç[HK1_TI_CMD_ENA/DIS]                  EQ      ENA
0201 C.          çç[HK1_TI_CMD_NUM]                      EQ      4
0202 C.          çç[HK1_NEXT_EXEC_PIM]                  EQ      DHU
0203 C.          çç[HK1_NEXT_EXEC_DC]                   EQ      0xB3
0204 C.
0205 C. *****
0206 C. TIİİ°èŷÄŷÖŷ×
0207 C. *****
0208 C.
0209 C. TI_TBL(0x03AB00-0x03AEFF;§ 1024byte)
0210 +. DC 01-23 DHU_DMA_DMP_PRM_SET
0211 BC      (03 ab 03 01 02)
0212 C.          çç[HK1_DMP_TOP_ADRS_1]                  EQ      07
0213 C.          çç[HK1_DMP_TOP_ADRS_0]                  EQ      2B
0214 C.          çç[HK1_DMP_BLOCK_NUM]                   EQ      3
0215 C.          çç[HK1_DMP_REPEAT_NUM]                  EQ      0
0216 C.          çç[HK1_DMA_DMP_PIM]                     EQ      DHU
0217 +. DC 01-22 DHU_MODE_CHNG
0218 BC      (07 0b f8)
0219 C.          çç[HK1_PKT_FORM_NO]                     EQ      7
0220 C.          çç[HK1_PKT_GEN_TIME]                     EQ      0.25 s
0221 C.          çç[HK1_S_TLM_BIT_RATE]                  EQ      32k
0222 C.          çç[HK1_X_TLM_BIT_RATE]                  EQ      4M
0223 C.          çç[HK1_DMP_CHK_FLG]                     EQ      EXEC
0224 C.
0225 C. ŷÄŷÖŷ×½ªİ»õ³İÇ§
0226 C.          çç[HK1_DMP_CHK_FLG]                     EQ      NON
0227 C.
0228 C. RAM ID=TI_TBLõİ½È¹ç•è²İOKõ³İÇ§
0229 C.
0230 C. DHUŷä;¼ŷÈ;È½ŷ¼. ŷİ;¼ŷÈ;Èõðİãõ¹
0231 +. DC 01-22 DHU_MODE_CHNG
0232 BC      (02 0a f8)
0233 C.          çç[HK1_PKT_FORM_NO]                     EQ      2
0234 C.          çç[HK1_PKT_GEN_TIME]                     EQ      0.5S
0235 C.          çç[HK1_S_TLM_BIT_RATE]                  EQ      32K
0236 C.          çç[HK1_X_TLM_BIT_RATE]                  EQ      4M
0237 C.
0238 C. *****
0239 C. SOT TI command set
0240 C. *****
0241 C. Execute, after the success of OP upload.
0242 +. TI 2014-10-30 10:18:16.0
0243 DC 07-F0 MDP_SOT_MODE_STBY
0244 BC      (41)
0245 C. -----
0246 C.   HK1_TI_CMD_NUM          = 1 CNTUP [ ]
0247 C. -----
0248 C. ***** SOT END *****
0249 C. Stop EIS observation and temporarily disable EIS mode changes
0250 C.
0251 C.
0252 C. ***** Start EIS operation (TI set) *****
0253 C. Execute, after the success of OP upload.
0254 C. Set EIS TI-commands
0255 +. TI 2014-10-30 10:18:30.0
0256 DC 07-FC EIS_MODE_MANU
0257 BC      (21 02)
0258 +. TI 2014-10-30 10:18:40.0
0259 DC 07-FC EIS_MODE_CHG_DIS
0260 BC      (22)
0261 C.          [ ] [HK1_TI_CMD_NUM]                      EQ      2 COUNTUP
0262 C. ***** End EIS operation (TI set) *****
0263 C.
0264 C.
0265 C.
0266 C. ***** XRT START *****
0267 C. Execute, after the success of OP upload.
0268 +. TI 2014-10-30 10:18:00.0
0269 DC 07-F0 MDP_XRT_MODE_STBY
0270 BC      (c3)
0271 C.          [ ] [HK1_TI_CMD_NUM]                      EQ      1COUNTUP
0272 C.
0273 C. ***** XRT END *****
0274 C.
0275 C. ***** MDP ´üÄİõİ»õ¼ŷõÈÄõ¹õÈDCBC•x²è *****
0276 C. (¼ªõİŷÖŷÄŷÈŷŷŷÄŷçŷèõÈ¼õõ¼Ä»Üõ¹õè)
0277 S. DC-BC dcbc-402:DCBC
0278 (MDP_known_event)
0279 C.
0280 C.
0281 C. ***** ŷĐŷ¹•İ Daily±çİñõÈ'Øõ¹õÈDCBC•x²è *****
0282 S. DC-BC dcbc-153:DCBC
0283 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0284 C.
0285 C.
0286 C. ;ãLOSŷÄŷ§ŷÄŷ-¼Ä»Ü;ã
0287 C.
0288 C. ***** LOS *****
0289 C.

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0096 C.
0097 C.
0098 . C. *****
0099 C. SOT table upload
0100 C. *****
0101 . C. < Stop FG table >
0102 +. DC 07-F0 MDP_FG_CTRL_MANU
0103 BC (51)
0104 . C. -----
0105 C. MDP_FG_CTRL_MODE = MANU [ ]
0106 C. -----
0107 C.
0108 . C. <Upload FG Observation Table>
0109 . S. RAM ram-267:MDP_OBS_F
0110 ( )
0111 C.
0112 . C. < Dump RAMID=MDP_OBS_F >
0113 +. DC 07-F0 MDP_DUMP_FGTBL
0114 BC (82 07 00 00 00 38 b8)
0115 C. -----
0116 C. MDP_OBS_F verify = OK/NG [ ]
0117 C. -----
0118 C.
0119 C. *****
0120 C. SOT TI command set
0121 C. *****
0122 C. Execute, after the success of TBL upload.
0123 +. TI 2014-10-30 10:18:18.0
0124 DC 07-F0 MDP_SOT_MODE_OBSV
0125 BC (40)
0126 . C. -----
0127 C. HK1_TI_CMD_NUM = 1 CNTUP [ ]
0128 C. -----
0129 C.
0130 C.
0131 C. ***** XRT START *****
0132 C.
0133 +. DC 07-F0 MDP_XRT_CTRL_MANU
0134 BC (c1)
0135 + DC 07-F0 MDP_XRT_MODE_STBY
0136 BC (c3)
0137 . C. ----- Success Verify ? OK / NG____
0138 C.
0139 C. XRT Obs. Table Upload
0140 . S. RAM ram-291:MDP_OBS_X
0141 ( )
0142 C.
0143 +. DC 07-F0 MDP_DUMP_XRTTBL
0144 BC (84 07 00 00 00 3a d4)
0145 . C. ----- Comparison Check ? OK / ERR ____
0146 C.
0147 C.
0148 +. DC 07-F0 MDP_XRT_ROI_SET
0149 BC (cd 01 b1 b1 04 04)
0150 + DC 07-F0 MDP_XRT_ROI_SET
0151 BC (cd 02 b1 b1 08 08)
0152 + DC 07-F0 MDP_XRT_ROI_SET
0153 BC (cd 03 b1 b1 08 08)
0154 + DC 07-F0 MDP_XRT_ROI_SET
0155 BC (cd 04 b1 b1 06 06)
0156 + DC 07-F0 MDP_XRT_ROI_SET
0157 BC (cd 05 85 83 06 06)
0158 + DC 07-F0 MDP_XRT_ROI_SET
0159 BC (cd 06 85 83 08 08)
0160 + DC 07-F0 MDP_XRT_ROI_SET
0161 BC (cd 07 85 83 06 06)
0162 + DC 07-F0 MDP_XRT_ROI_SET
0163 BC (cd 08 80 80 20 20)
0164 + DC 07-F0 MDP_XRT_ROI_SET
0165 BC (cd 09 80 80 20 08)
0166 + DC 07-F0 MDP_XRT_ROI_SET
0167 BC (cd 0a 80 80 08 20)
0168 + DC 07-F0 MDP_XRT_ROI_SET
0169 BC (cd 0f 80 80 06 06)
0170 + DC 07-F0 MDP_XRT_ROI_SET
0171 BC (cd 10 80 80 08 08)
0172 + DC 07-F0 MDP_XRT_FLD_ENA
0173 BC (d8)
0174 + DC 07-F0 MDP_XRT_FLRCTRL_ENA
0175 BC (c8)
0176 + DC 07-F0 MDP_XRT_AEC_RESET
0177 BC (d0)
0178 + DC 07-F0 MDP_XRT_ARS_DIS
0179 BC (d5)
0180 + DC 07-F0 MDP_XRT_FLD_RESET
0181 BC (da)
0182 +. DC 07-F0 MDP_XRT_QT_PROG_SET
0183 BC (c4 06)
0184 +. DC 07-F0 MDP_XRT_FL_PROG_SET
0185 BC (c5 01)
0186 . C. ----- Success Verify ? OK / NG ____
0187 C.
0188 C.
0189 . C. All OK? Yes--> Please Proceed. / No --> Stop here.
0190 C.
0191 +. DC 07-F0 MDP_XRT_MODE_OBSV
0192 BC (c2)
0193 +. TI 2014-10-30 10:18:02.0

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0194 DC 07-F0 MDP_XRT_MODE_OBSV
0195 BC (c2)
0196 . C. ----- Success Verify ? OK / NG ____
0197 C.
0198 C. ***** XRT END *****
0199 C.
0200 . C. ***** MDP `úÃîñî»ò¼ŷñÊÂĐñ¹ñèDCBC•x²è *****
0201 C. (¼á°îŷÓŷÃŷÈŷŦŷËŷáŷçŷèñÊ¼ñ¼Ã»Ûñ¹ñè)
0202 . S. DC-BC dcbc-402:DCBC
0203 (MDP_known_event)
0204 C.
0205 C.
0206 . C. ***** ŷĐŷ¹•İ Daily±¿İÑñÊ´Øñ¹ñèDCBC•x²è *****
0207 . S. DC-BC dcbc-153:DCBC
0208 (SPECIAL-CMD_DAILY_OPERATIN_DCB)
0209 C.
0210 C.
0211 . C. ;ãLOSŷÁŷŦŷËŷ¹¼Ã»Ûñ¹ñè
0212 C.
0213 . C. ***** LOS *****
0214 C.
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\*\*\* OP Sequence for XRT \*\*\*

2014/10/30	10:28:54.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	10:28:56.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	10:28:58.0	XRT_FOCUS_POSITION_410_OG [0x19a]					
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00		
2014/10/30	10:29:00.0	AOCS_Ore-point_Start_1_OG [0x097]					
		AOCU_NM	5	02-76	00 18 72 b0 fe		
2014/10/30	10:29:18.0	XRT_FLD_ENA_411_OG [0x19b]					
		MDP_XRT_FLD_ENA	1	07-F0	d8		
2014/10/30	10:29:20.0	XRT_FLRCTRL_ENA_412_OG [0x19c]					
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8		
2014/10/30	10:29:22.0	XRT_AEC_RESET_413_OG [0x19d]					
		MDP_XRT_AEC_RESET	1	07-F0	d0		
2014/10/30	10:29:24.0	XRT_ARS_DIS_423_OG [0x1a7]					
		MDP_XRT_ARS_DIS	1	07-F0	d5		
2014/10/30	10:29:26.0	XRT_FLD_RESET_407_OG [0x197]					
		MDP_XRT_FLD_RESET	1	07-F0	da		
2014/10/30	10:31:56.0	XRT_QT_PROG_SET_440_OG [0x1b8]					
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d		
2014/10/30	10:31:58.0	XRT_FL_PROG_SET_438_OG [0x1b6]					
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 01		
2014/10/30	10:32:00.0	XRT_CTRL_AUTO_408_OG [0x198]					
		MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2014/10/30	12:00:00.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	12:00:02.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	12:00:04.0	XRT_FOCUS_POSITION_410_OG [0x19a]					
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00		
2014/10/30	12:00:24.0	XRT_FLD_ENA_411_OG [0x19b]					
		MDP_XRT_FLD_ENA	1	07-F0	d8		
2014/10/30	12:00:26.0	XRT_FLRCTRL_ENA_412_OG [0x19c]					
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8		
2014/10/30	12:00:28.0	XRT_AEC_RESET_413_OG [0x19d]					
		MDP_XRT_AEC_RESET	1	07-F0	d0		
2014/10/30	12:00:30.0	XRT_ARS_DIS_423_OG [0x1a7]					
		MDP_XRT_ARS_DIS	1	07-F0	d5		
2014/10/30	12:00:32.0	XRT_FLD_RESET_407_OG [0x197]					
		MDP_XRT_FLD_RESET	1	07-F0	da		
2014/10/30	12:03:02.0	XRT_QT_PROG_SET_433_OG [0x1b1]					
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 04		
2014/10/30	12:03:04.0	XRT_FL_PROG_SET_438_OG [0x1b6]					
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 01		
2014/10/30	12:03:06.0	XRT_CTRL_AUTO_408_OG [0x198]					
		MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2014/10/30	14:06:00.0	XRT_CTRL_MANU_400_OG [0x190]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	14:06:02.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	14:06:04.0	XRT_FLD_RESET_415_OG [0x19f]					
		MDP_XRT_FLD_RESET	1	07-F0	da		
2014/10/30	14:06:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]					
		MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2014/10/30	14:09:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]					
		MDP_XRT_PREFLR_STOP	1	07-F0	e9		
2014/10/30	14:12:00.0	XRT_Custom_430_OG [0x1ae]					
2014/10/30	14:13:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
		MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2014/10/30	15:00:00.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	15:00:02.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	15:00:04.0	XRT_FOCUS_POSITION_410_OG [0x19a]					
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00		
2014/10/30	15:00:24.0	XRT_FLD_ENA_411_OG [0x19b]					
		MDP_XRT_FLD_ENA	1	07-F0	d8		
2014/10/30	15:00:26.0	XRT_FLRCTRL_ENA_412_OG [0x19c]					
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8		
2014/10/30	15:00:28.0	XRT_AEC_RESET_413_OG [0x19d]					
		MDP_XRT_AEC_RESET	1	07-F0	d0		
2014/10/30	15:00:30.0	XRT_ARS_DIS_423_OG [0x1a7]					
		MDP_XRT_ARS_DIS	1	07-F0	d5		
2014/10/30	15:00:32.0	XRT_FLD_RESET_407_OG [0x197]					
		MDP_XRT_FLD_RESET	1	07-F0	da		
2014/10/30	15:03:02.0	XRT_QT_PROG_SET_440_OG [0x1b8]					
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d		
2014/10/30	15:03:04.0	XRT_FL_PROG_SET_438_OG [0x1b6]					
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 01		
2014/10/30	15:03:06.0	XRT_CTRL_AUTO_408_OG [0x198]					
		MDP_XRT_CTRL_AUTO	1	07-F0	c0		
2014/10/30	15:38:30.0	XRT_CTRL_MANU_400_OG [0x190]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	15:38:32.0	XRT_CTRL_MANU_402_OG [0x192]					
		MDP_XRT_CTRL_MANU	1	07-F0	c1		
2014/10/30	15:38:34.0	XRT_FLD_RESET_415_OG [0x19f]					
		MDP_XRT_FLD_RESET	1	07-F0	da		
2014/10/30	15:38:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]					
		MDP_XRT_PREFLR_STRT	1	07-F0	e8		
2014/10/30	15:41:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]					
		MDP_XRT_PREFLR_STOP	1	07-F0	e9		

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2014/10/30	16:02:00.0	XRT_Custom_430_OG [0x1ae]			
2014/10/30	16:03:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	17:15:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	17:15:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	17:15:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/30	17:15:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/30	17:18:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/30	17:38:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/30	17:39:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	17:55:54.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	17:55:56.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	17:55:58.0	XRT_FOCUS_POSITION_403_OG [0x193]			
		XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00
2014/10/30	17:56:00.0	AOCS_OrE-point_Start_2_OG [0x098]			
		AOCU_NM	5	02-76	00 00 00 00 00
2014/10/30	17:56:18.0	XRT_FLD_DIS_422_OG [0x1a6]			
		MDP_XRT_FLD_DIS	1	07-F0	d9
2014/10/30	17:58:54.0	XRT_FLRCTRL_DIS_405_OG [0x195]			
		MDP_XRT_FLRCTRL_DIS	1	07-F0	c9
2014/10/30	17:58:56.0	XRT_ARS_DIS_423_OG [0x1a7]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2014/10/30	17:58:58.0	XRT_QT_PROG_SET_420_OG [0x1a4]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 05
2014/10/30	17:59:00.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	18:05:54.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	18:05:56.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	18:05:58.0	XRT_FOCUS_POSITION_410_OG [0x19a]			
		XRT_FOCUS_POSITION	4	07-F8	22 fe 97 00
2014/10/30	18:06:00.0	AOCS_OrE-point_Start_1_OG [0x097]			
		AOCU_NM	5	02-76	00 18 72 b0 fe
2014/10/30	18:06:18.0	XRT_FLD_ENA_411_OG [0x19b]			
		MDP_XRT_FLD_ENA	1	07-F0	d8
2014/10/30	18:06:20.0	XRT_FLRCTRL_ENA_412_OG [0x19c]			
		MDP_XRT_FLRCTRL_ENA	1	07-F0	c8
2014/10/30	18:06:22.0	XRT_AEC_RESET_413_OG [0x19d]			
		MDP_XRT_AEC_RESET	1	07-F0	d0
2014/10/30	18:06:24.0	XRT_ARS_DIS_423_OG [0x1a7]			
		MDP_XRT_ARS_DIS	1	07-F0	d5
2014/10/30	18:06:26.0	XRT_FLD_RESET_407_OG [0x197]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/30	18:08:56.0	XRT_QT_PROG_SET_440_OG [0x1b8]			
		MDP_XRT_QT_PROG_SET	2	07-F0	c4 0d
2014/10/30	18:08:58.0	XRT_FL_PROG_SET_438_OG [0x1b6]			
		MDP_XRT_FL_PROG_SET	2	07-F0	c5 01
2014/10/30	18:09:00.0	XRT_CTRL_AUTO_408_OG [0x198]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	18:52:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	18:52:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	18:52:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/30	18:52:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/30	18:55:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/30	19:15:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/30	19:16:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	20:29:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	20:29:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	20:29:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/30	20:29:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/30	20:32:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/30	20:52:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/30	20:53:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/30	22:07:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	22:07:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/30	22:07:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/30	22:07:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/30	22:10:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			

2014/10/30	22:28:30.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/30	22:29:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/30	23:44:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/30	23:44:02.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/30	23:44:04.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/30	23:44:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/10/30	23:47:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/10/30	23:54:00.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/30	23:55:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/31	01:09:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	01:09:32.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	01:09:34.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	01:09:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/10/31	01:12:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/10/31	01:27:00.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/31	01:28:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/31	02:43:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	02:43:02.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	02:43:04.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	02:43:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/10/31	02:46:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/10/31	03:03:30.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/31	03:04:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/31	04:12:00.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	04:12:02.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	04:12:04.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	04:12:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/10/31	04:15:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/10/31	04:41:00.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/31	04:42:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/31	05:52:30.0	XRT_CTRL_MANU_400_OG [0x190]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	05:52:32.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	05:52:34.0	XRT_FLD_RESET_415_OG [0x19f]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	05:52:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]	MDP_XRT_FLD_RESET	1	07-F0	da	
2014/10/31	05:55:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]	MDP_XRT_PREFLR_STRT	1	07-F0	e8	
2014/10/31	06:18:30.0	XRT_Custom_430_OG [0x1ae]	MDP_XRT_PREFLR_STOP	1	07-F0	e9	
2014/10/31	06:19:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]					
2014/10/31	06:28:24.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	06:28:26.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	06:28:28.0	XRT_FOCUS_POSITION_403_OG [0x193]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31	06:28:30.0	AOCS_Ore-point_Start_2_OG [0x098]	XRT_FOCUS_POSITION	4	07-F8	22 ff aa 00	
2014/10/31	06:28:48.0	XRT_FLD_DIS_422_OG [0x1a6]	AOCU_NM	5	02-76	00 00 00 00 00	
2014/10/31	06:31:24.0	XRT_FLRCTRL_DIS_405_OG [0x195]	MDP_XRT_FLD_DIS	1	07-F0	d9	
2014/10/31	06:31:26.0	XRT_ARS_DIS_423_OG [0x1a7]	MDP_XRT_FLRCTRL_DIS	1	07-F0	c9	
2014/10/31	06:31:28.0	XRT_QT_PROG_SET_420_OG [0x1a4]	MDP_XRT_ARS_DIS	1	07-F0	d5	
2014/10/31	06:31:30.0	XRT_CTRL_AUTO_408_OG [0x198]	MDP_XRT_QT_PROG_SET	2	07-F0	c4 05	
2014/10/31	06:38:30.0	AOCS_Ore-point_Start_1_OG [0x097]	MDP_XRT_CTRL_AUTO	1	07-F0	c0	
2014/10/31	06:39:00.0	XRT_CTRL_MANU_402_OG [0x192]	AOCU_NM	5	02-76	00 18 72 b0 fe	
2014/10/31	06:39:02.0	XRT_CTRL_MANU_402_OG [0x192]	MDP_XRT_CTRL_MANU	1	07-F0	c1	
2014/10/31			MDP_XRT_CTRL_MANU	1	07-F0	c1	



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2014/10/31	06:40:00.0	XRT_TCIB_XRT_S_HTR_A_ENA_446_OG [0x1be]			
		TCIB_XRT_S_HTR_A_ENA	0	04-BC	
2014/10/31	07:32:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	07:32:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	07:32:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	07:32:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	07:35:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	07:55:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	07:56:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	09:12:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	09:12:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	09:12:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	09:12:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	09:15:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	09:31:00.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	09:32:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	14:39:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	14:39:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	14:39:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	14:39:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	14:42:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	14:50:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	14:51:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	16:14:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	16:14:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	16:14:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	16:14:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	16:17:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	16:37:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	16:38:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	17:51:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	17:51:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	17:51:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	17:51:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	17:54:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	18:14:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	18:15:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	19:28:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	19:28:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	19:28:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	19:28:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	19:31:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	19:51:00.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	19:52:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/10/31	21:05:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	21:05:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	21:05:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	21:05:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	21:08:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	21:28:30.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	21:29:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0

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2014/10/31	22:42:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	22:42:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/10/31	22:42:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/10/31	22:42:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/10/31	22:45:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/10/31	23:03:00.0	XRT_Custom_430_OG [0x1ae]			
2014/10/31	23:04:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	00:20:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	00:20:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	00:20:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	00:20:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	00:23:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	00:27:00.0	XRT_Custom_430_OG [0x1ae]			
2014/11/01	00:28:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	01:43:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	01:43:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	01:43:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	01:43:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	01:46:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	02:02:30.0	XRT_Custom_430_OG [0x1ae]			
2014/11/01	02:03:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	03:18:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	03:18:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	03:18:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	03:18:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	03:21:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	03:39:30.0	XRT_Custom_430_OG [0x1ae]			
2014/11/01	03:40:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	04:49:00.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	04:49:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	04:49:04.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	04:49:06.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	04:52:14.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	05:17:00.0	XRT_Custom_430_OG [0x1ae]			
2014/11/01	05:18:00.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	06:29:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	06:29:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	06:29:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	06:29:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	06:32:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	06:54:30.0	XRT_Custom_430_OG [0x1ae]			
2014/11/01	06:55:30.0	XRT_CTRL_AUTO_424_OG [0x1a8]			
		MDP_XRT_CTRL_AUTO	1	07-F0	c0
2014/11/01	08:09:30.0	XRT_CTRL_MANU_400_OG [0x190]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	08:09:32.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	08:09:34.0	XRT_FLD_RESET_415_OG [0x19f]			
		MDP_XRT_FLD_RESET	1	07-F0	da
2014/11/01	08:09:36.0	XRT_PREFLR_STRT_439_OG [0x1b7]			
		MDP_XRT_PREFLR_STRT	1	07-F0	e8
2014/11/01	08:12:44.0	XRT_PREFLR_STOP_419_OG [0x1a3]			
		MDP_XRT_PREFLR_STOP	1	07-F0	e9
2014/11/01	09:30:00.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	09:30:02.0	XRT_CTRL_MANU_402_OG [0x192]			
		MDP_XRT_CTRL_MANU	1	07-F0	c1
2014/11/01	09:50:00.0	AOCS_Ore-point_Start_2_OG [0x098]			

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5 02-76 00 00 00 00 00